

# Iris 14"/15" Schematics

## Bay Trail - M

2014-11-11

REV : A00

*DY : None Installed*

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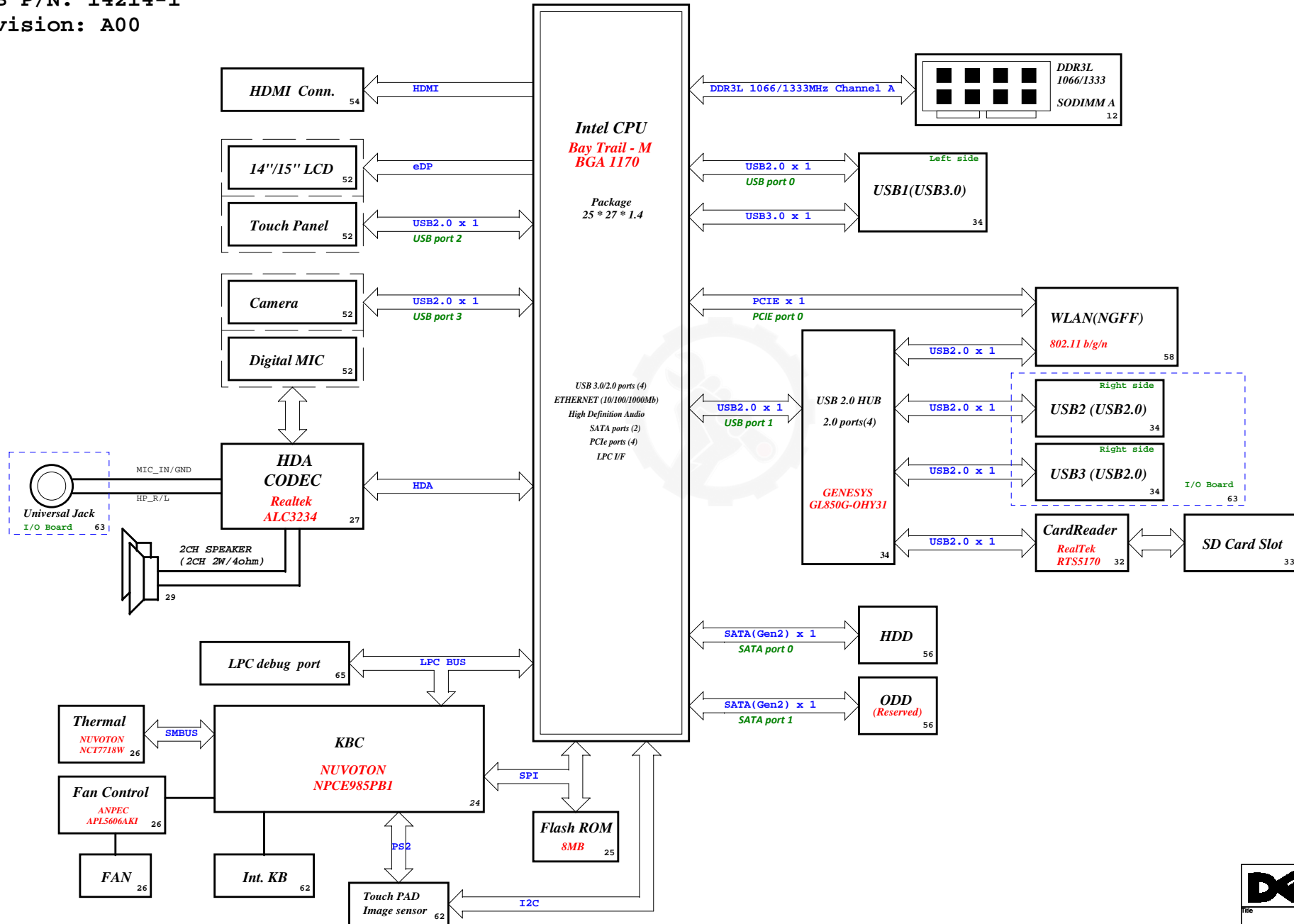
Title		
Cover Page		
Size A3	Document Number Iris BTM	Rev A00
Date: Tuesday, November 11, 2014	Sheet 1	of 102

Project code:  
4PD02V010001 (14")  
4PD030010001 (15")

PCB P/N: 14214-1  
Revision: A00

# Iris Bay Trail-M Block Diagram

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CHARGER	
BQ24727RGRR-1-GP 44	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT
SYSTEM DC/DC	
TPS51225RUKR-GP 45	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5
CPU Core Power	
ISL95833HRTZ-GP 46,47	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
DDR3L SUS	
TPS51716RUKR-GP 49	
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D675V_S0
CPU 1.05V	
SY8206DQNC-GP-U 50	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0
CPU 1.0V	
RT9041E-12GQW-GP 51	
INPUTS	OUTPUTS
3D3V_S5	1D0V_S5
System LDO 1.8V	
S-1339D18-M5T1U3-GP 51	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5
System LDO 1.5V	
S-1339D15-M5001-GP 51	
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
System switches	
INPUTS	OUTPUTS
5V_S5	5V_S0
3D3V_S5	3D3V_S0
1D8V_S5	1D8V_S0
1D35V_S3	1D35V_S0
PCB LAYER	
L1:Top L2:GND L3:Signal L4:Signal L5:VCC L6:Bottom	


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Main Func = CPU

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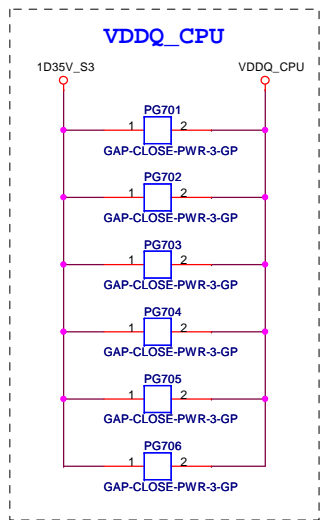
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**Iris BTM**

Rev  
**A00**

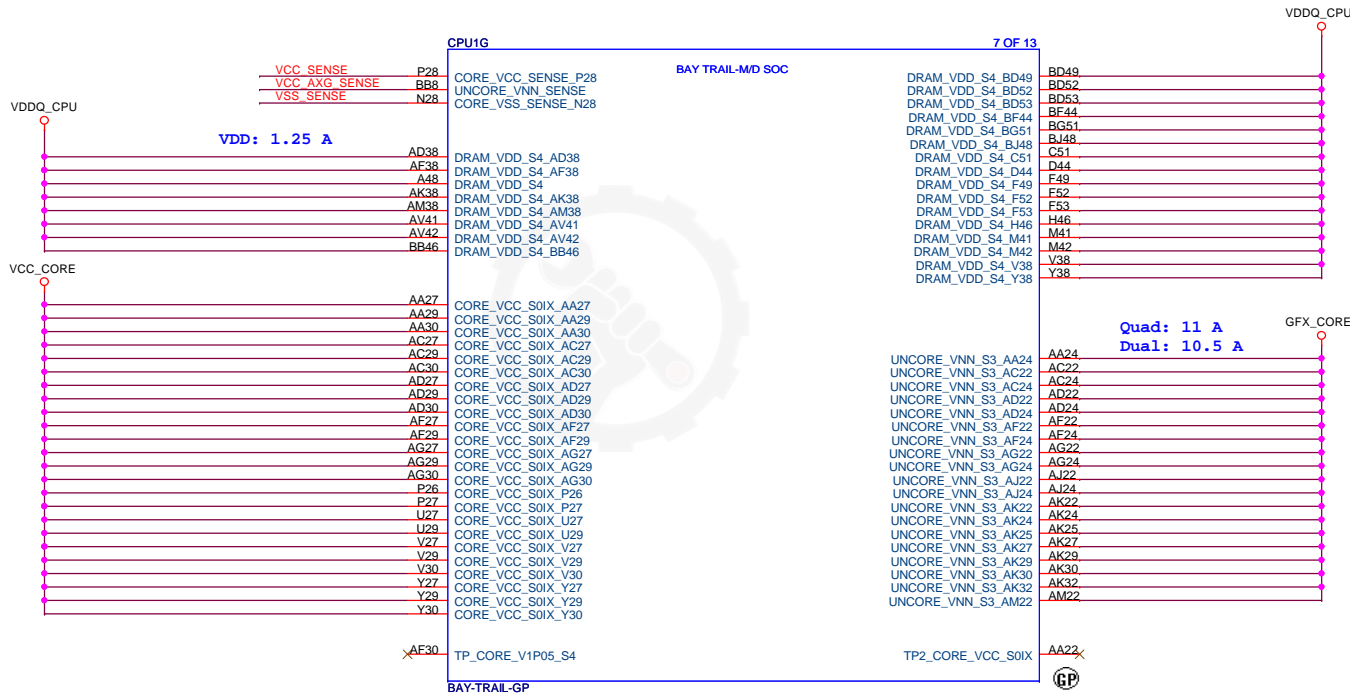
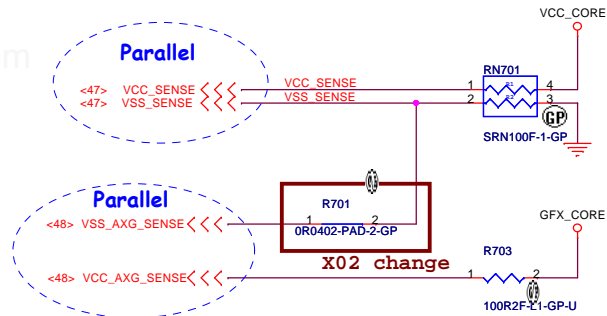
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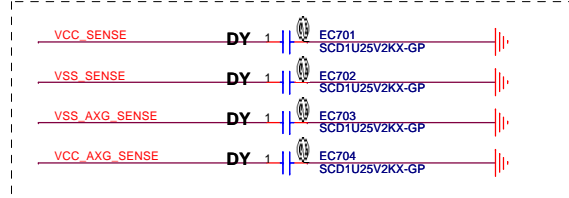
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### EMI Caps.



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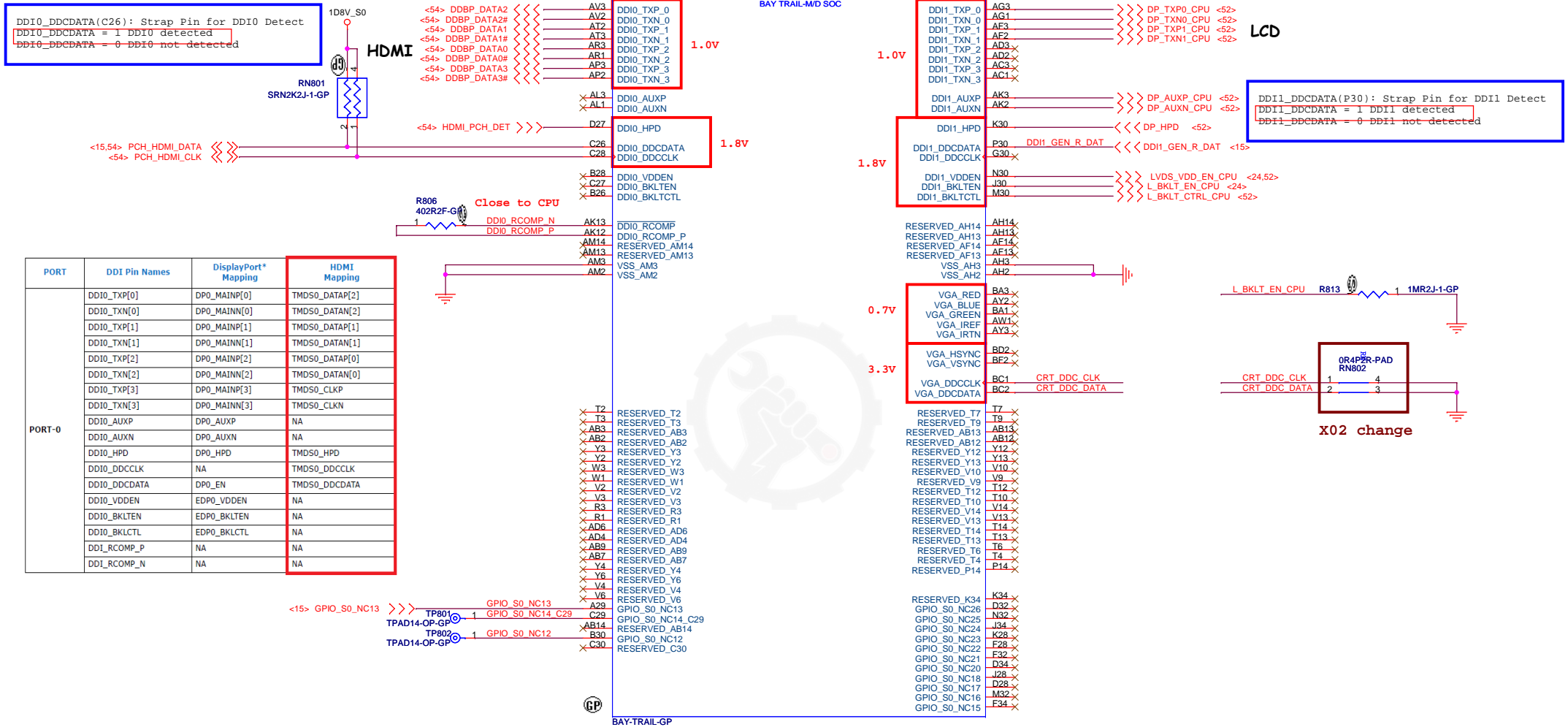
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Size			Document Number		
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Main Func = CPU

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DDI0\_DDCDATA(C26): Strap Pin for DDI0 Detect  
DDI0\_DDCDATA = 1 DDI0 detected  
DDI0\_DDCDATA = 0 DDI0 not detected

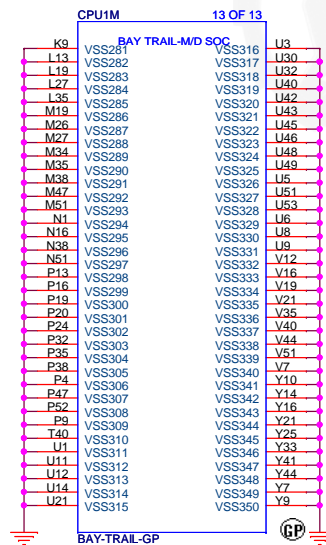
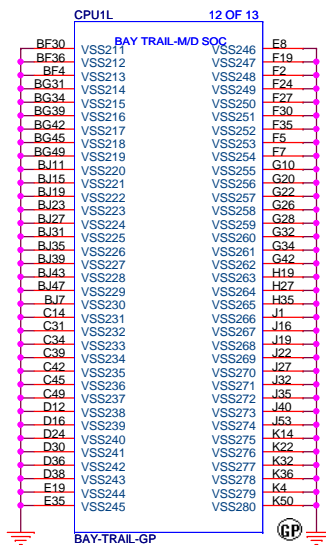
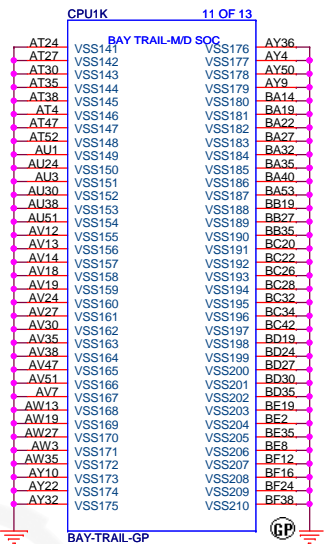
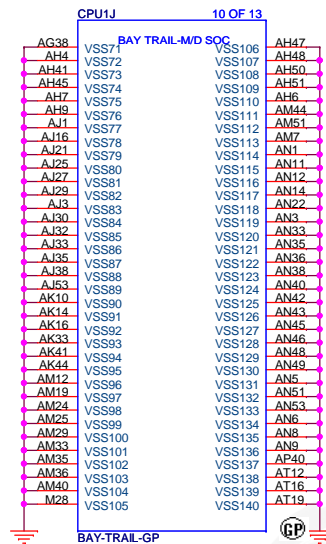
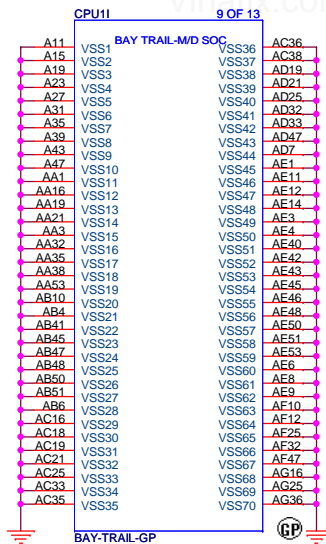


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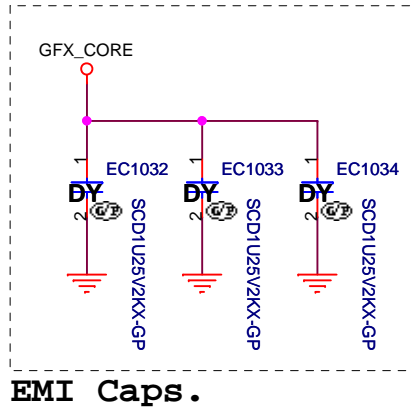
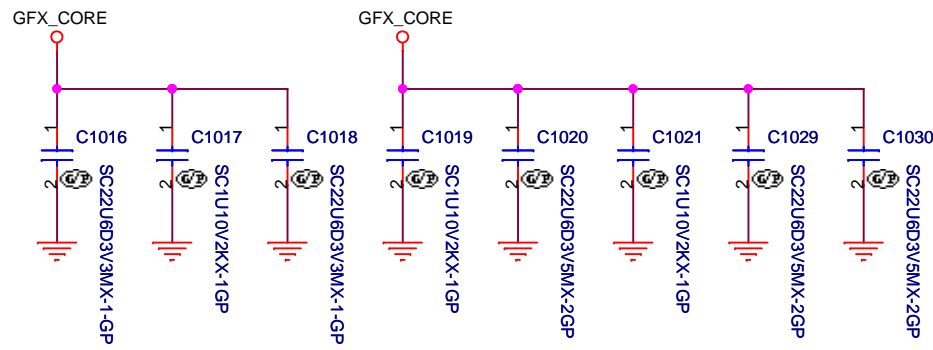
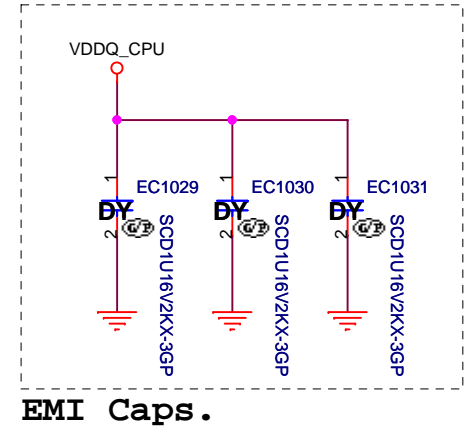
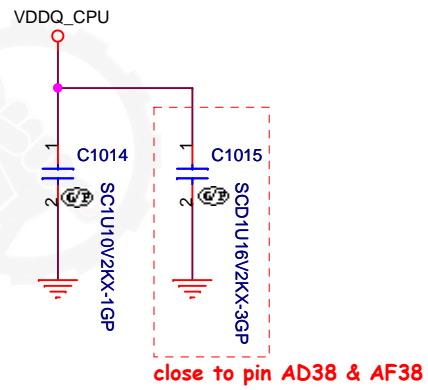
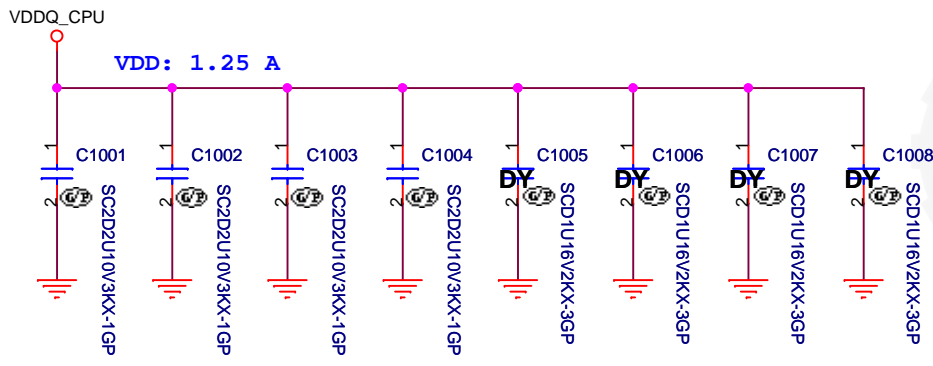
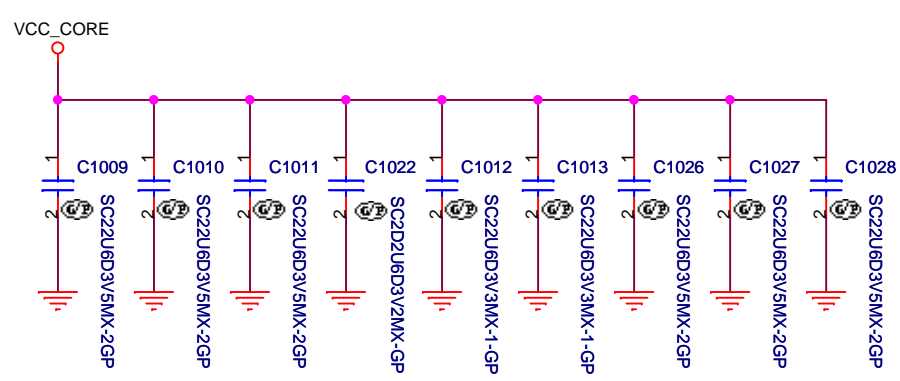
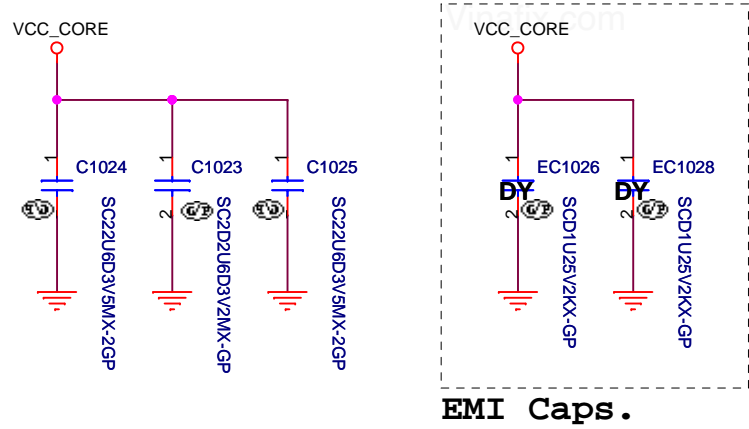
Title CPU (DDI/EDP/GPIO)  
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Main Func = CPU



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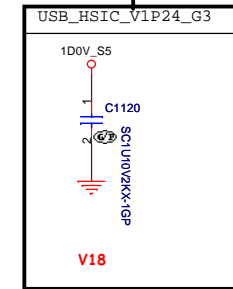
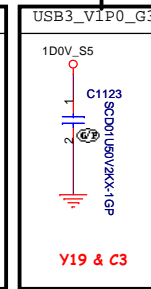
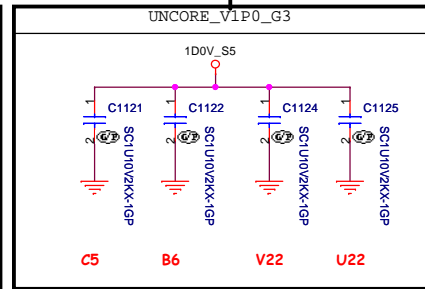
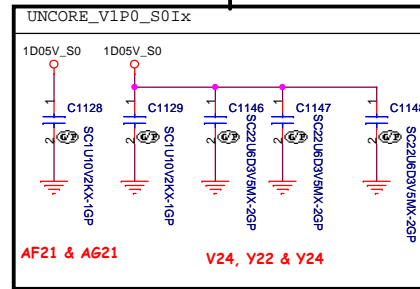
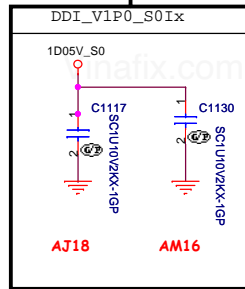
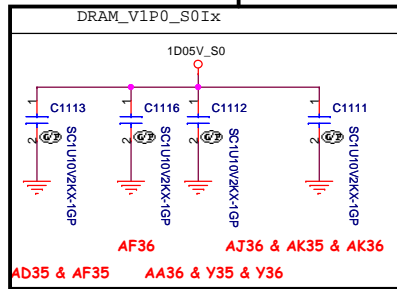
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Size A4	Document Number <b>Iris BTM</b>	Rev <b>A00</b>
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# Main Func = CPU

VLP0Sx: 2.1 A

VLP0A: 0.35 A

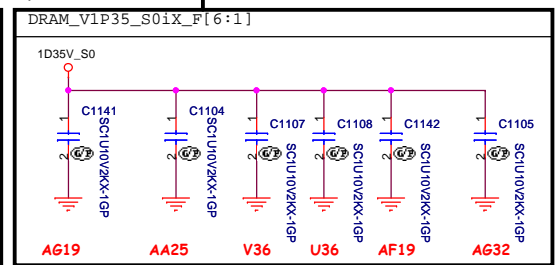
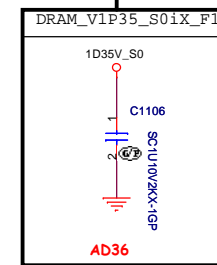
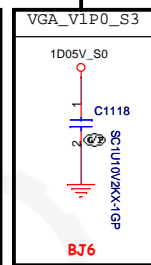
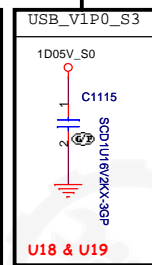
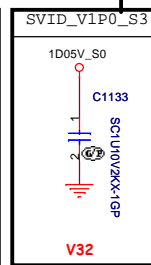
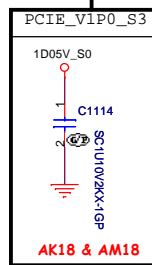
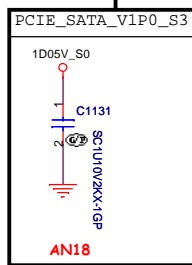
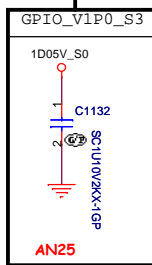
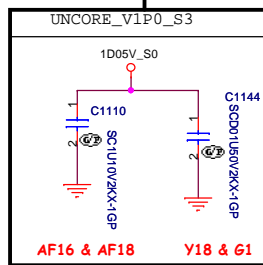
VLP24A: 0.035 A



V18: USB\_HSIC\_VLP24\_G3 pin(s) can be connected to VLP0A platform rail if USB HSIC is not used.

VLP0S: 0.9 A

VLP35Sx (VSFR): 0.4 A

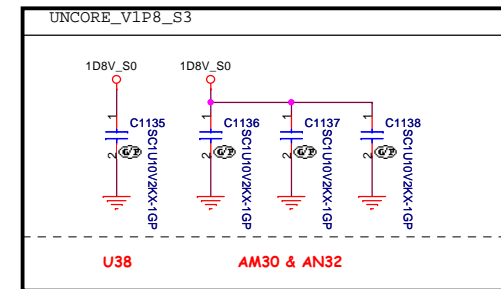
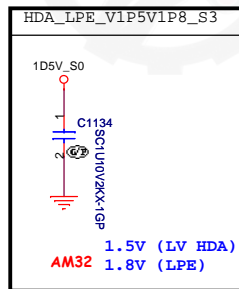
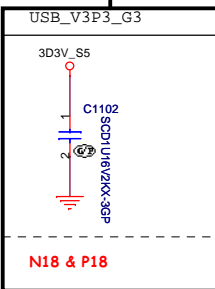
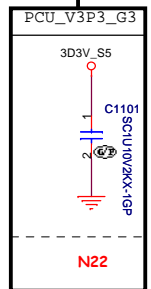
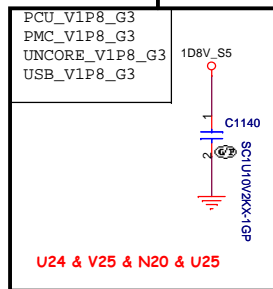
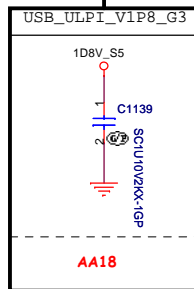


VLP8A: 0.065 A

V3P3A: 0.055 A

VLP5VLP8S (VAUD):  
See VLP8S

VLP8S: 0.01 A

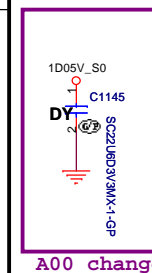
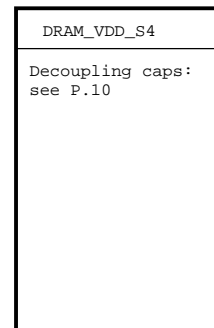
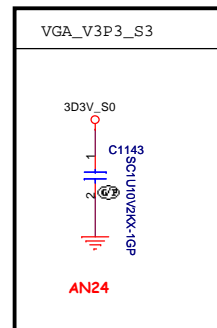
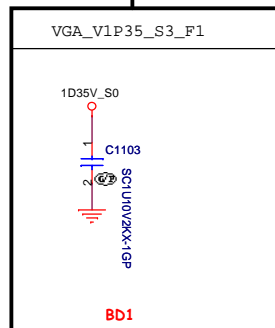
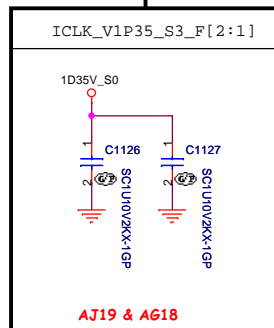
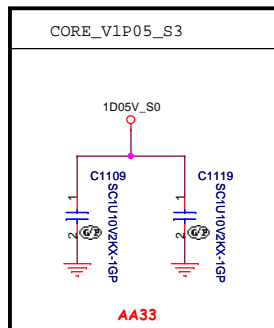


VLP05S: 1.1 A

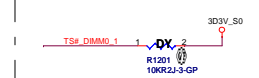
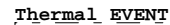
VLP35S: 0.045 A

V3P3S: 0.03 A

VDD: 1.25 A

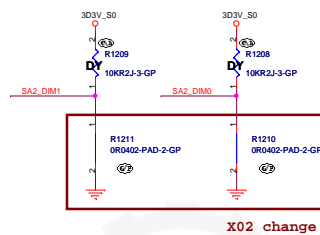


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**Note:**  
If SA0\_DIM0 = 0, SA1\_DIM0 = 0  
SO-DIMMA SPD Address is 0xA0  
SO-DIMMA TS Address is 0x30

If SA0\_DIM0 = 1, SA1\_DIM0 = 0  
SO-DIMMA SPD Address is 0xA2  
SO-DIMMA TS Address is 0x32



x02 change

Decoupling caps: one 0.1 uF placed close to VREF pins of each DDR3 SODIMM.

```
| Decoupling caps: one 0.1 uF placed close to
| VREF pins of each DDR3 SODIMM.
```

10V5V\_S3

C1203 C1204 C1205 C1206 C1207 C1221 C1222 C1223

SC10A010200-10P SC10A010200-10P SC10A010200-10P SC10A010200-10P SC10A010200-10P SC10A010200-10P SC10A010200-10P SC10A010200-10P

C1209 C1210 C1211 C1212

SC10U01200-10P SC10U01200-10P SC10U01200-10P SC10U01200-10P

Layout Note:  
Place these Caps near SO-DIMMA.

#509653	check list recommend
10uF * 8	
0.1uF * 8	

Layout Note:  
Place these Caps near SO-DIMMA.

```
#509653 check list recommend
10uF * 8
0.1uF * 8
```

0603V50

C1214 C1215 C1216 C1217 C1219 C1220

Place these caps close to VTT1 and VTT2.

509653 check list recomm  
1uF \* 4  
10uF \* 2

Place these caps  
close to VTT1 and VTT2.

```
#509653 check list recommend
1uF * 4
10uF * 2
```


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Main Func = DIMM1

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Main Func = DIMM1

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Main Func = PCH

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC  
SHOULD BE PLACED OUTSIDE KOZ AREA

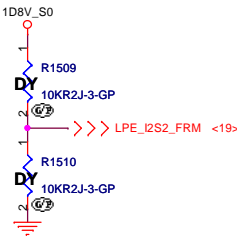
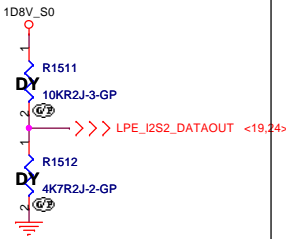
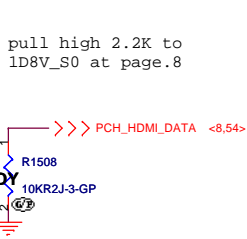
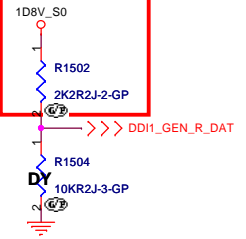
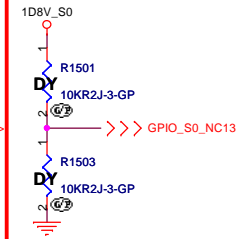
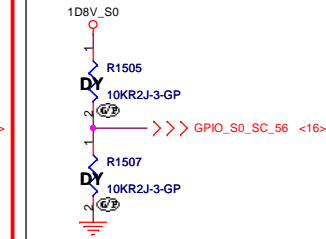
Description	BIOS Boot Selection	Security Flash Descriptors	DDI0 Detect	DDI1 Detect	DDI1 Detect	Top swap (A16 Override)
GPIO	GPIO_S0_SC[063]	GPIO_S0_SC[065]	DDI0_DDCDATA	DDI1_DDCDATA	MDSI_DDCDATA	GPIO_S0_SC [56]
Schematic						
High	SPI (Default)	Normal Operation (Default)	DDI0 detected	DDI1 detected	DDI1 detected	Top address bit is unchanged (Default)
Low	LPC	Override	DDI0 not detected (Default)	DDI1 not detected (Default)	DDI1 not detected	Top address bit is inverted

Table 20. Straps

Signal Name	Function	Default	Strap Exit	Strap Description
GPIO_S0_SC[056]	Legacy	1b	PMC_CORE_PWROK de-asserted	Top Swap (A16 Override) 0 = Top address bit is inverted 1 = Top address bit is unchanged
GPIO_S0_SC[063]	Legacy	1b	PMC_CORE_PWROK de-asserted	BIOS Boot Selection 0 = LPC 1 = SPI
GPIO_S0_SC[065]	Legacy	1b	PMC_CORE_PWROK de-asserted	Security Flash Descriptors 0 = Override 1 = Normal Operation
DDI0_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected

INTEL BTM EDS Rev2.5

## 30.2 LPE\_I2S2\_DATAOUT/ GPIO\_S0\_SC[065]ball as Flash Descriptor Security Override

In order to update the entire flash during manufacturing process or as part of a board return flow, the flash Descriptor Security override ball BC30 (GPIO\_S0\_SC[065]) can be used to unlock the entire SPI flash (override descriptor setting) and to stop the Intel® TXE from accessing SPI.

For full description and implementation data, please refer to the Bay Trail M/D "Manufacturing Recommendations" document, CDI #515108, section #2.6.

### 27.1.1.2 Hardware Controlled

System hardware, external to the SoC, can be used to assert or de-assert the Top-Swap strapping input signal. If the signal is sampled as being asserted during power-up then Top-Swap is active.

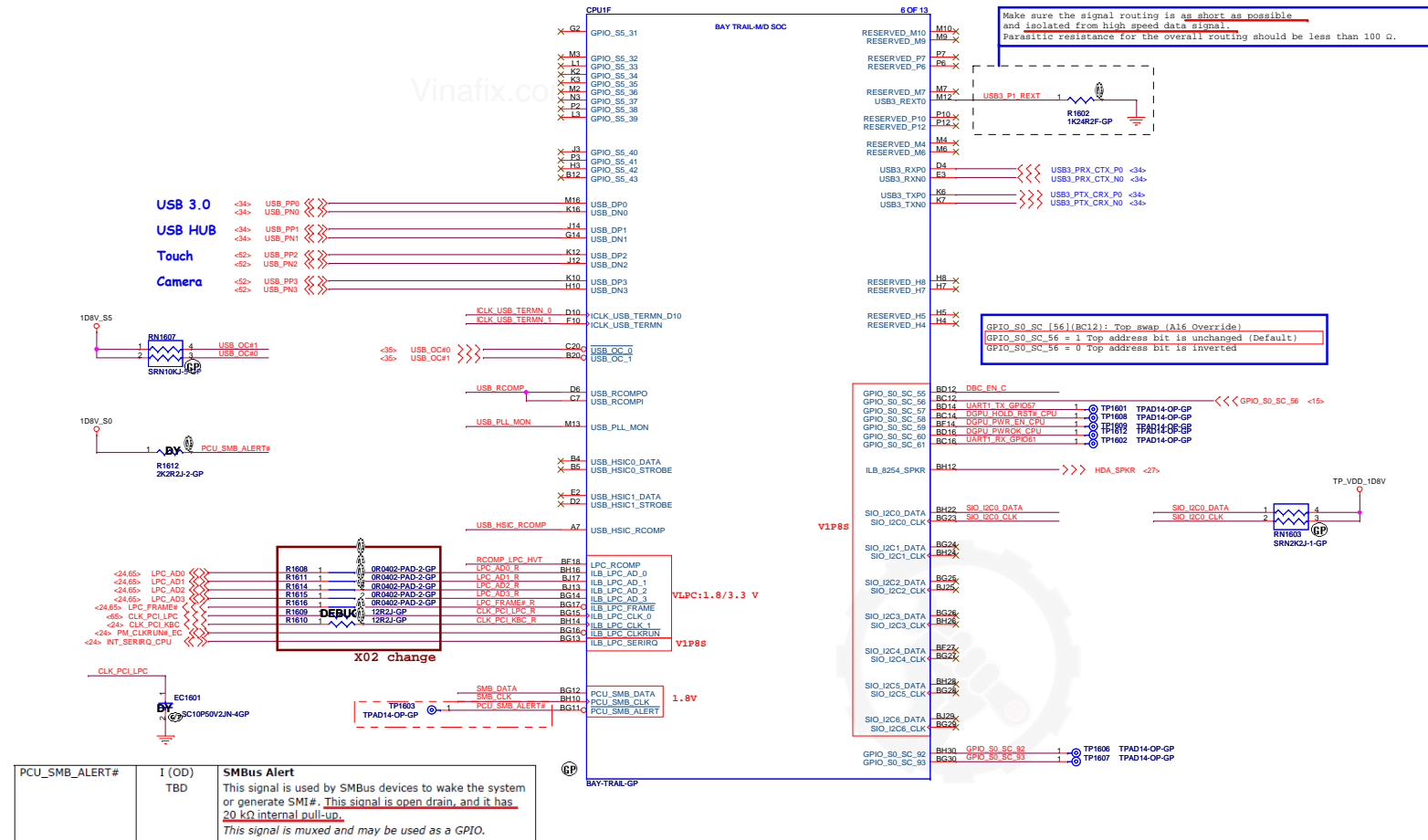
**Note:** The Top-Swap strap is an active high signal and is multiplexed with the GPIO\_S0\_SC[56] signal.

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Title			CPU (STRAP)	
Size A3	Document Number	Iris BTM		Rev A00
Date: Monday, November 17, 2014	Sheet 15	of 102		

# Main Func = PCH



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Main Func = PCH

Vinafix.com

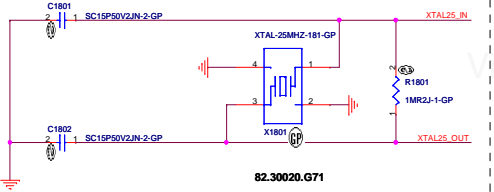
Blanking

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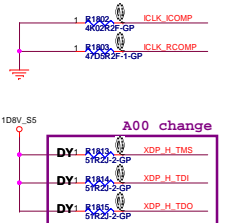
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)</b>			
Size A4	Document Number <b>Iris BTM</b>		Rev <b>A00</b>
Date: Tuesday, November 11, 2014		Sheet 17 of	102

Main Func = PCH

Crystal: 25 MHz



EE Note:  
C1801 and C1802:  
Select the capacitance base on the crystal measurement result.

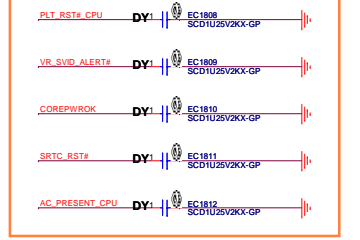


Layout Note:  
1. PLACE R1806, R1813, R1814 WITHIN 1.1" FROM SOC PIN  
2. PLACE R1815 WITHIN 0.25" FROM XDP PIN



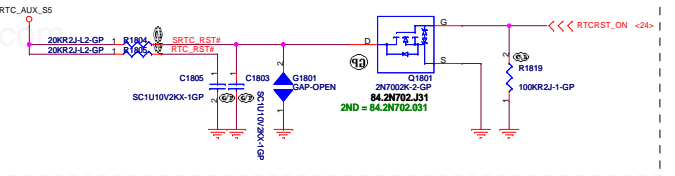
If no PCI Express ports is implemented on the platform pull-up to V1P8 Via a 10-KΩ resistor.

reserve the 0402 0.1u caps for EMI



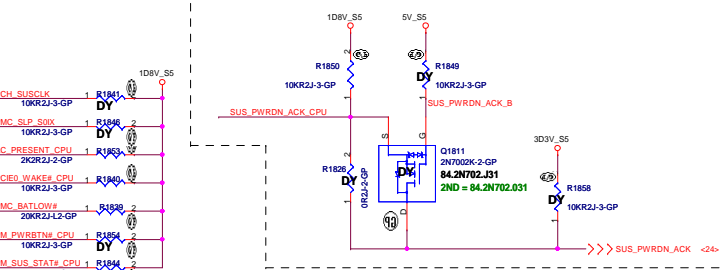
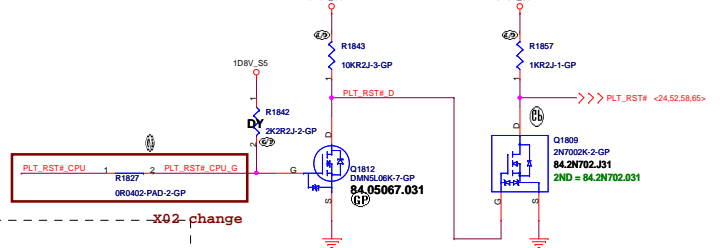
RTC Reset

ILB\_RTC\_RST#(RTC\_RST#):  
The signal input must always be high when all other RTC power planes are on.  
ILB\_RTC\_TEST#(SRTC\_RST#):  
The RC time delay should be in the 10-20 ms.

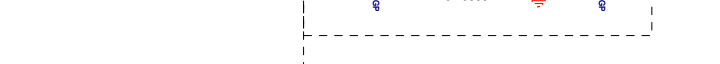
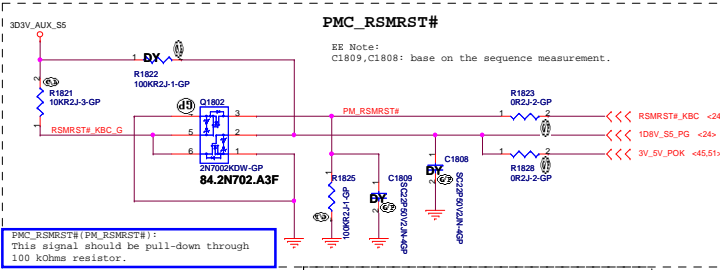


Level shift

EE Note:  
R1857: base on the Measurement of PL7\_RST#.

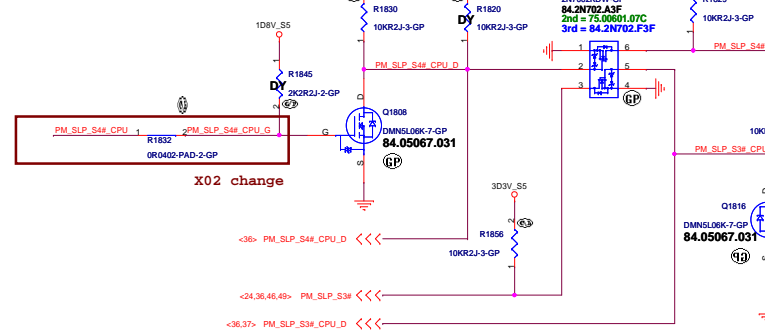


PM\_PWBRTN\_CPU (PM\_PWBRTN#):  
This signal has an internal pull-up resistor and has an internal ~16 ms de-bounce on the input.



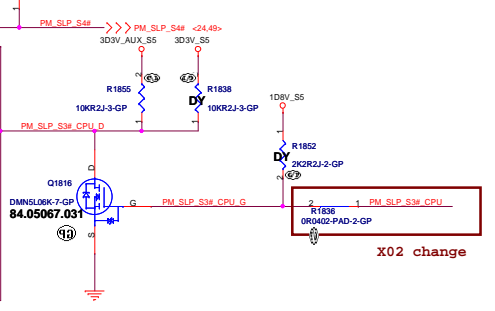
PMC\_SLP\_S4#

This signal is for power plane control. It can be used to control system power when it is in a S4 (Suspend to Disk) or S5 (Soft Off) state.

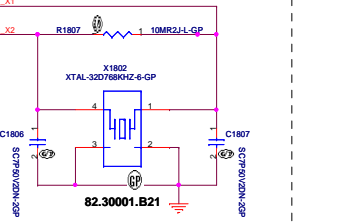


PMC\_SLP\_S3#

This signal is for power plane control. It can be used to control system power when it is in a S3 (Suspend to RAM), S4 (Suspend to Disk), or S5 (Soft Off) states.

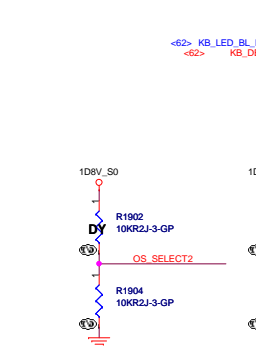
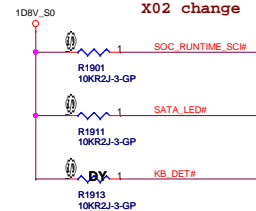
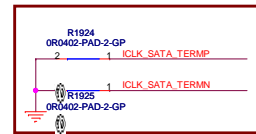


Crystal: 32.768 kHz



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# Main Func = PCH



	Win8.1	Android	Dual OS
OS_SELECT1	0	1	0
OS_SELECT2	0	0	1

	GPU_PRINT#
1	UMA
0	DIS

SATA\_GP:  
When used as an interlock switch status indication, this signal should be driven to '0' to indicate that the switch is closed, and to '1' to indicate that the switch is open.

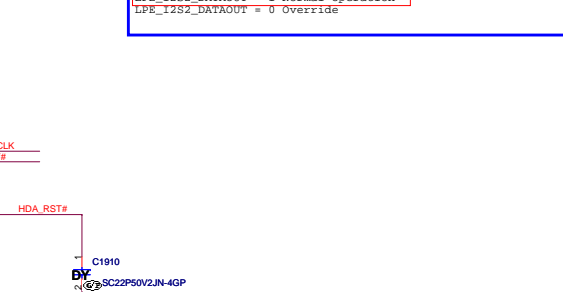
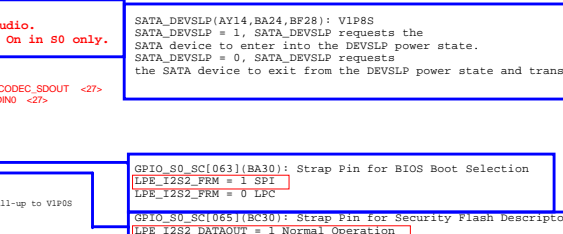
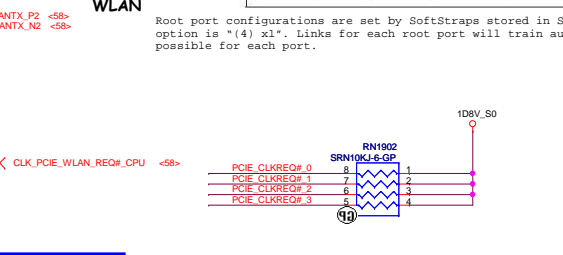
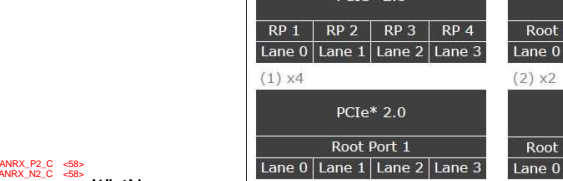
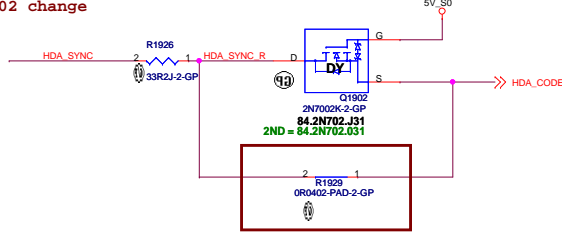
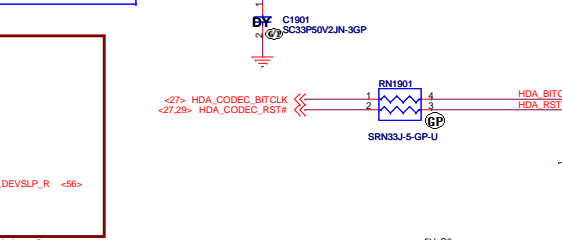
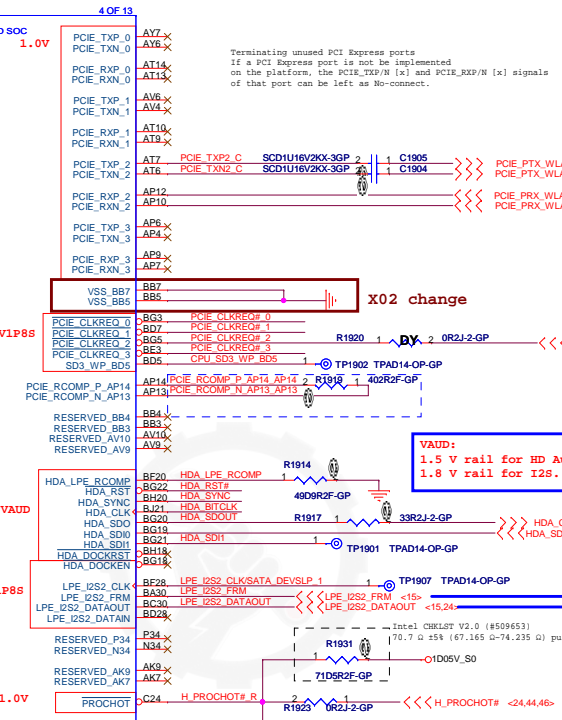
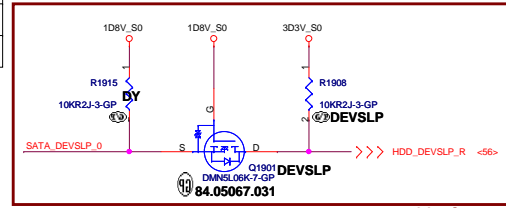
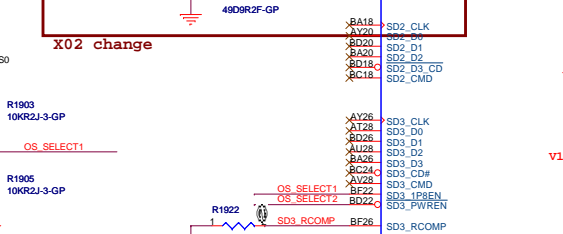
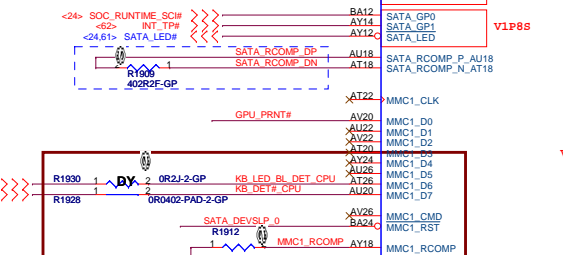
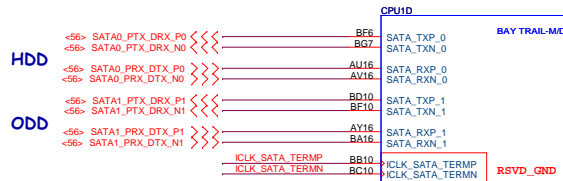
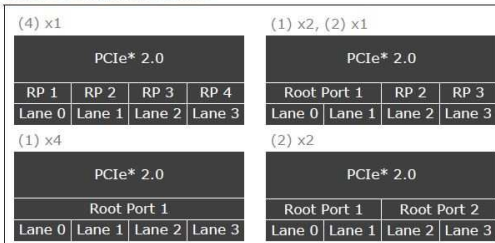
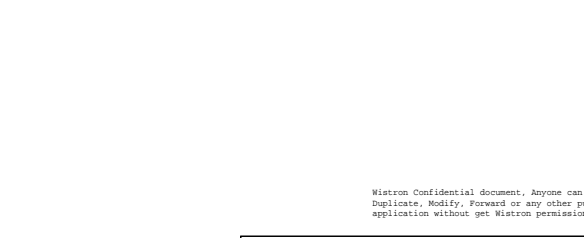
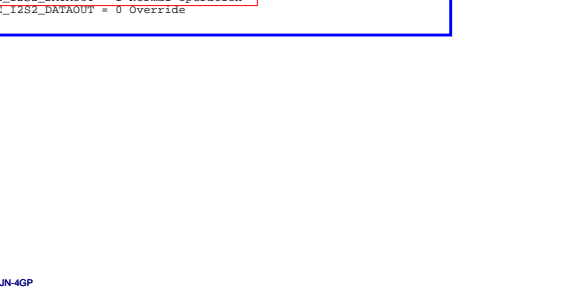
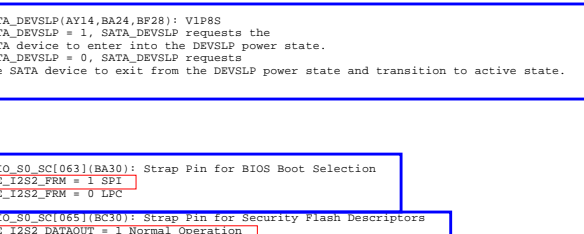
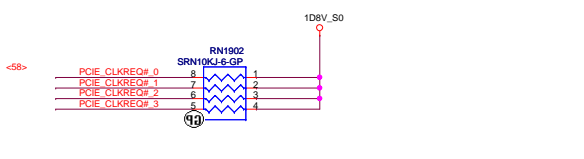


Figure 96. Root Port Configuration Options



Root port configurations are set by SoftStraps stored in SPI flash, and the default option is "(4) x1". Links for each root port will train automatically to the maximum possible for each port.



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Main Func = PCH

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Main Func = PCH

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Date: Tuesday, November 11, 2014		Sheet 22 of	102


Main Func = PCH

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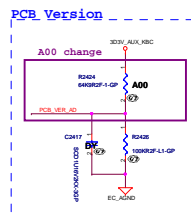
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Title <b>(Reserved)</b>			
Size A4	Document Number <b>Iris BTM</b>		Rev <b>A00</b>
Date: Tuesday, November 11, 2014		Sheet 23 of	102

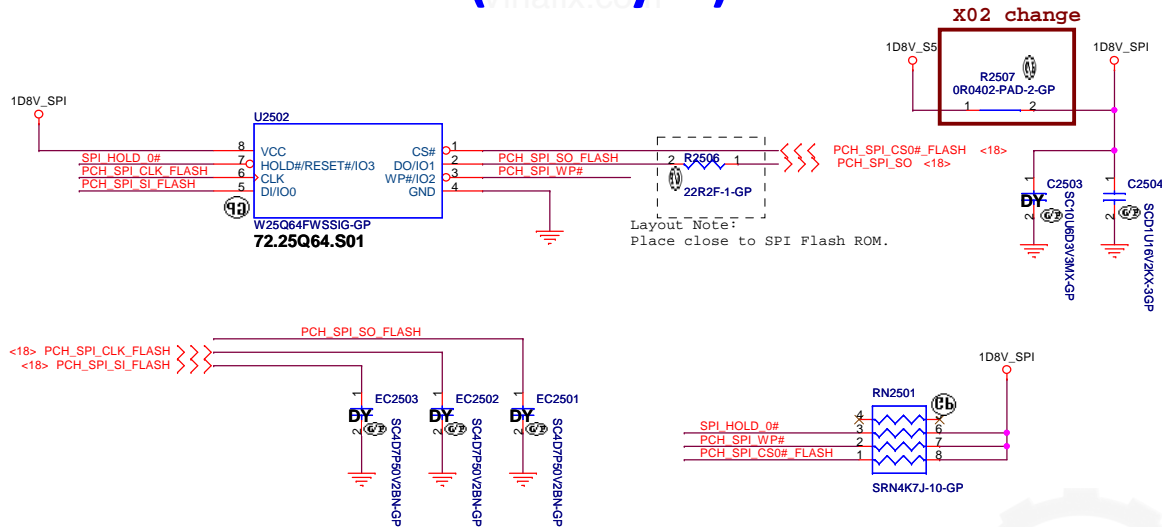
1

[illegible]



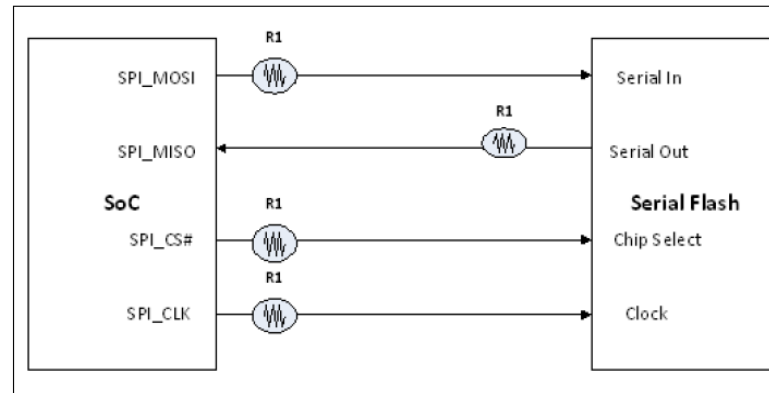
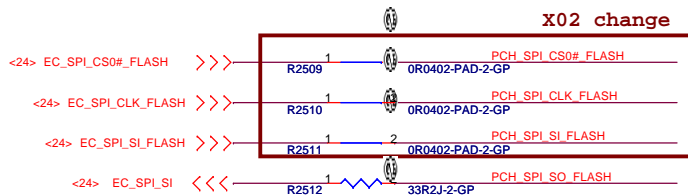
Main Func = SPI Flash

## SPI FLASH ROM (8M byte) for CPU



X02 change

## SPI ROM link to KBC



### NOTES:

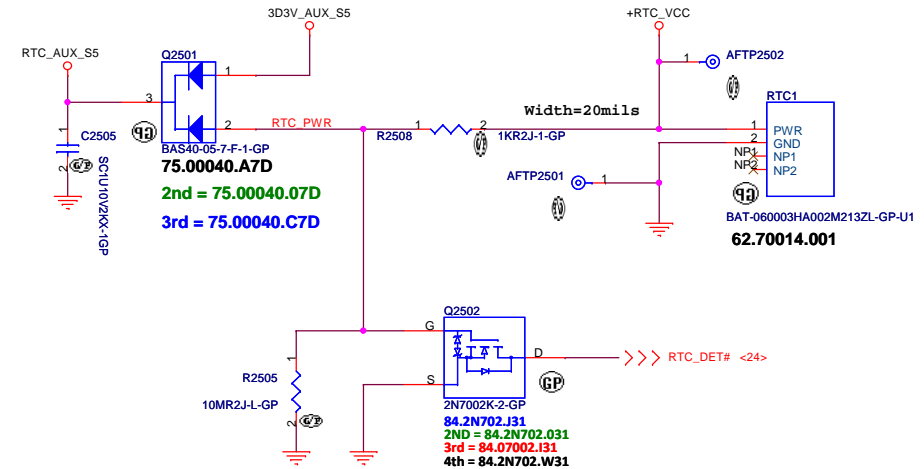
1. R1 = 22  $\Omega$  should be placed close to the SoC for SPI\_MOSI, SPI\_MOSI and SPI\_CLK signals.
2. R1 = 22  $\Omega$  should be placed close to the Serial Flash IC for SPI\_MISO signal

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Main Func = RTC

## RTC Battery

RTC coin cell  
23.20068.001



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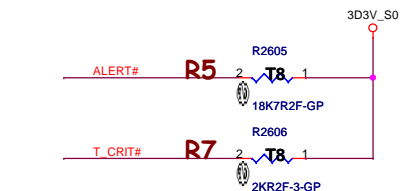
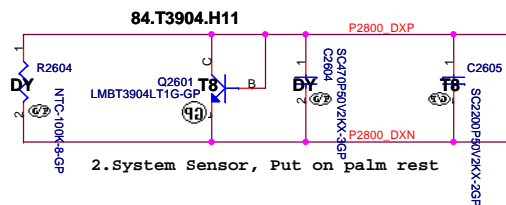
Title			Flash(KBC+PCH)/RTC	
Size	Document Number	Iris BTM		Rev
A3				A00
Date:	Monday, November 17, 2014	Sheet	25	of 102

Main Func = Thermal Sensor

EE Note:

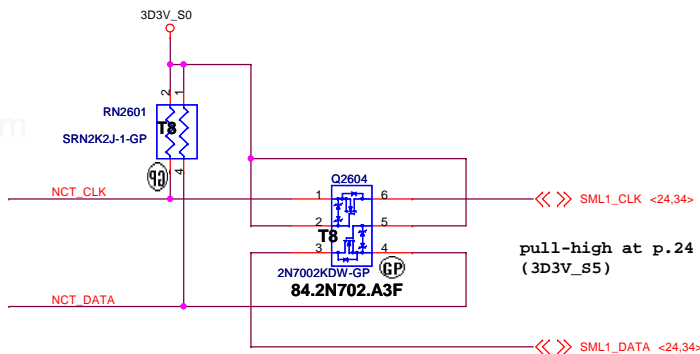
1. PURE\_KBCT8: PURE\_HW\_SHUTDOWN# w/o through Q2603.
2. T8: PURE\_HW\_SHUTDOWN# through Q2603.
3. THM\_SENSOR: Thermal sensor NCT7718W solution.  
(Need to stuff R2601 and DY R2602 for THERM\_SYS\_SHDN#)

Layout notice :  
Both DXN and DXP routing 10 mil  
trace width and 10 mil spacing.



The default value is trapping after power up 100ms by different pull-up resistors of T\_CRIT# and ALERT# pin:

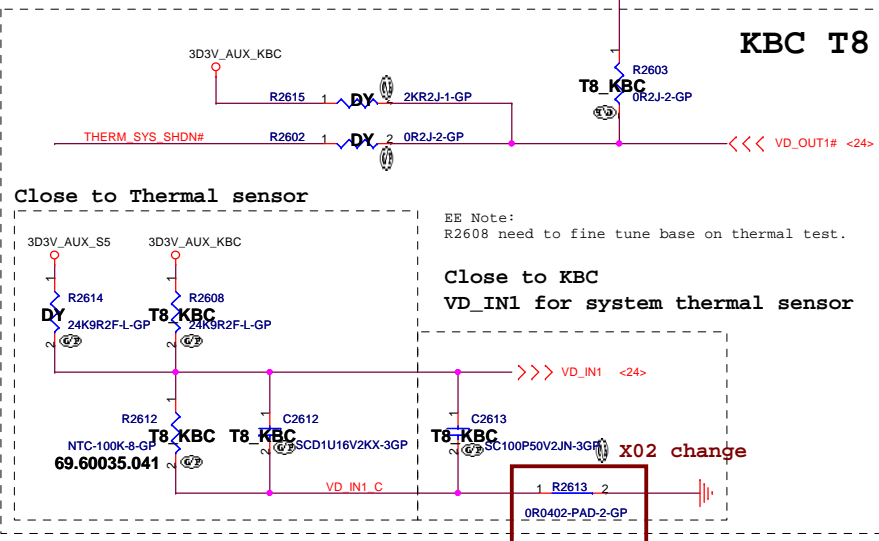
TEMPERATURE (°C)	T_CRIT#				
	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107
	7.5KΩ	79	89	99	109
	10.5KΩ	81	91	101	111
	14KΩ	83	93	103	113
	18.7KΩ	85	95	105	115



pull-high at p.24  
(3D3V\_S5)

Layout Note:  
Signal Routing Guideline:  
Trace width = 15mil

Thermal sensor NCT 7718W

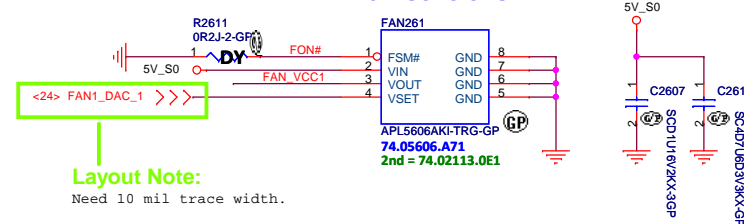


EE Note:  
R2608 need to fine tune base on thermal test.

Close to KBC  
VD\_IN1 for system thermal sensor

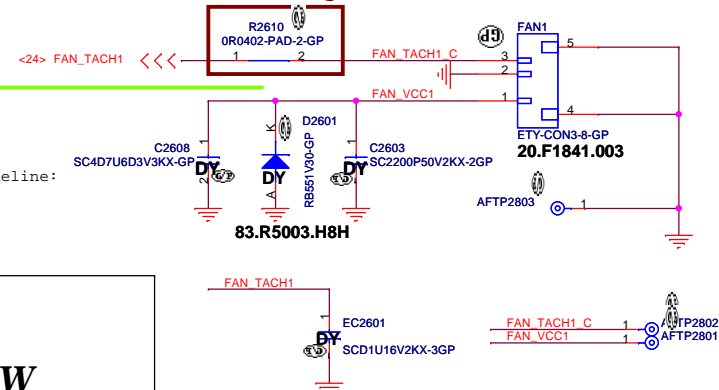
KBC T8

Fan controller1

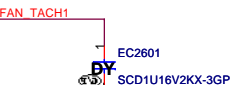


Layout Note:  
Need 10 mil trace width.

X02 change



83.R5003.H8H

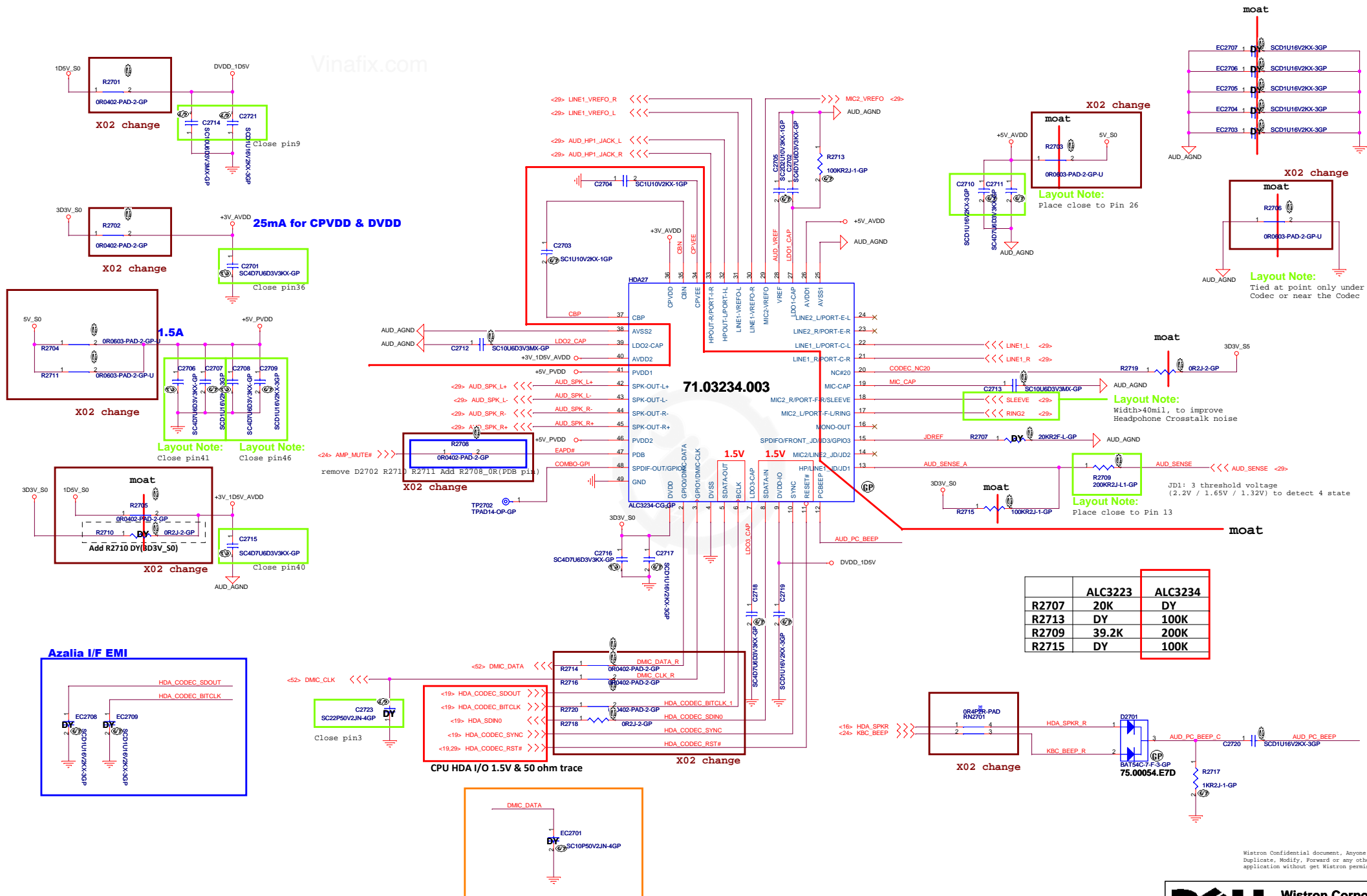


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Title: Thermal/Fan control  
Size: A3 Document Number: Iris BTM Rev: A00  
Date: Monday, November 17, 2014 Sheet: 26 of 102


**Main Func = Audio**



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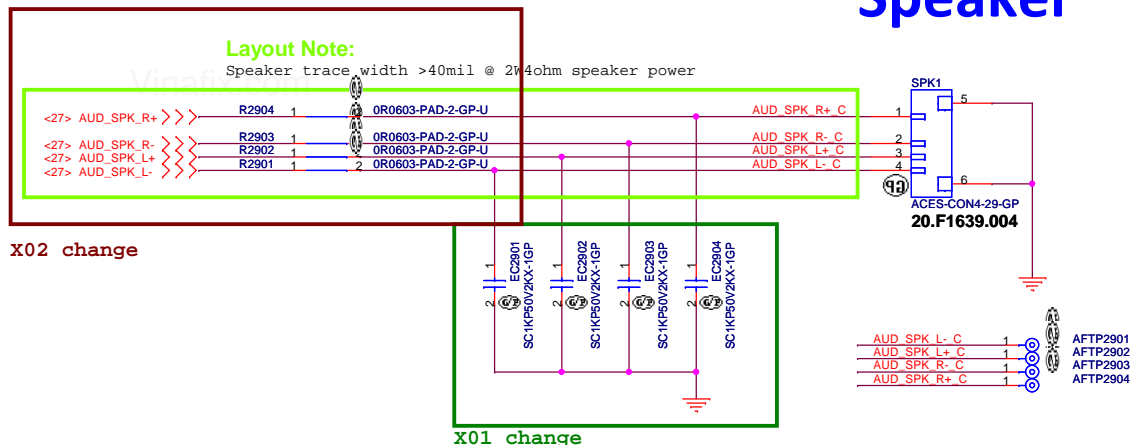
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Title <b>(Reserved)</b>			
Size A4	Document Number <b>Iris BTM</b>		Rev <b>A00</b>
Date: Tuesday, November 11, 2014		Sheet 28	of 102

Main Func = Audio

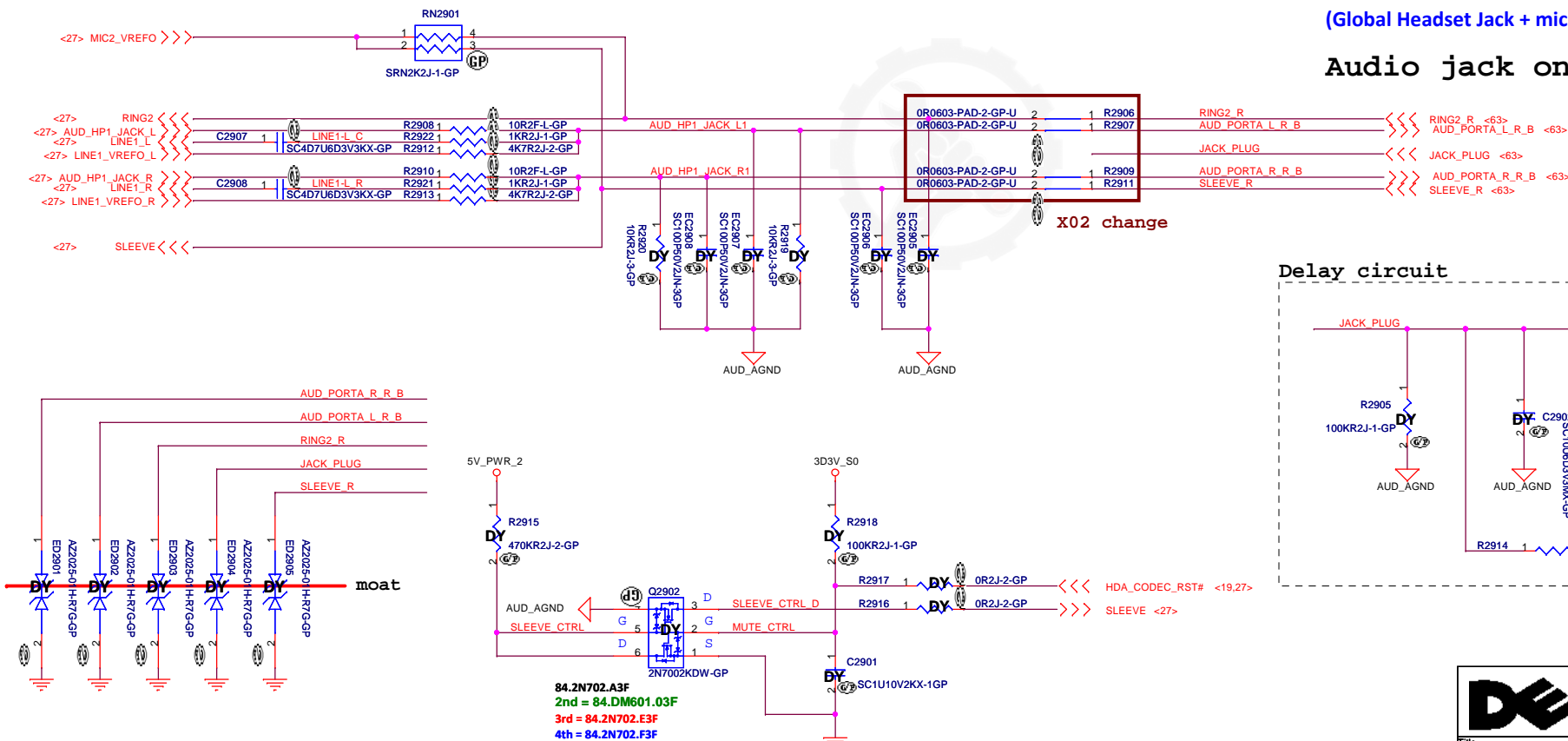
# Speaker



Main Func = Audio

Universal Jack  
(Global Headset Jack + mic phone in + line in support)

Audio jack on I/O Board.



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Title: **MIC/SPEAKER/AUDIOJACK**  
Size: Custom  
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Rev: **A00**  
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Main Func = LAN

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Main Func = LAN

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Title

(Reserved)

Size  
A4

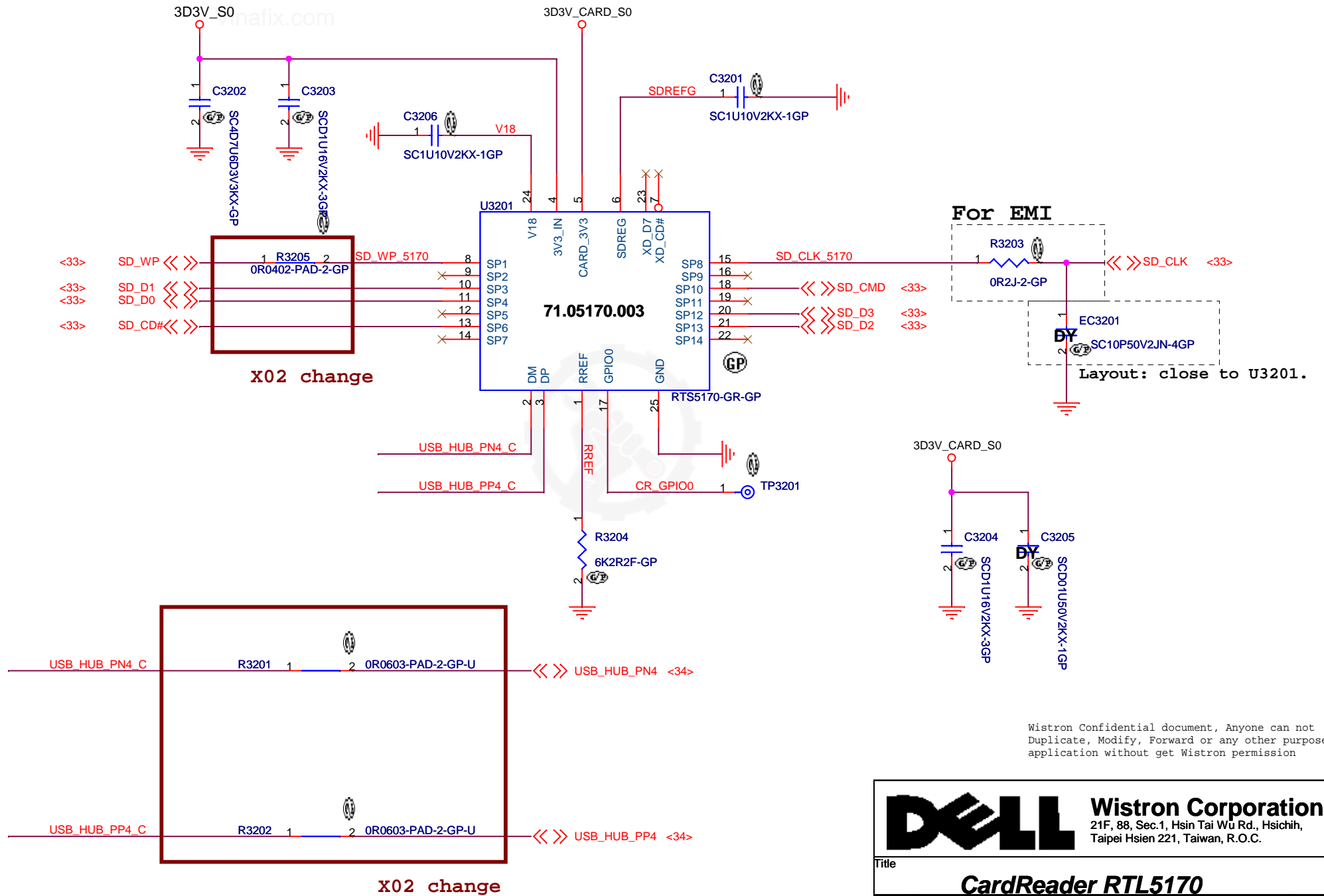
Document Number  
**Iris BTM**

Rev  
**A00**

Date: Tuesday, November 11, 2014

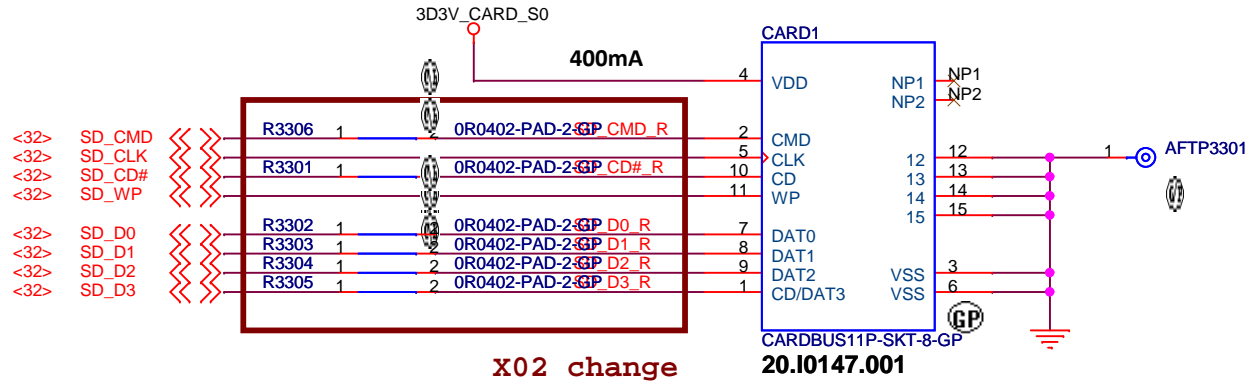
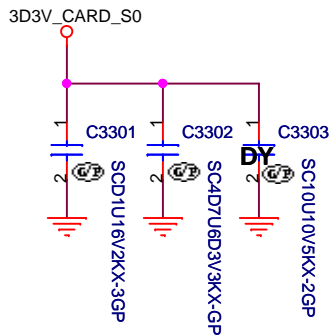
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# Main Func = Card Reader

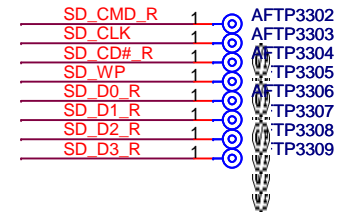
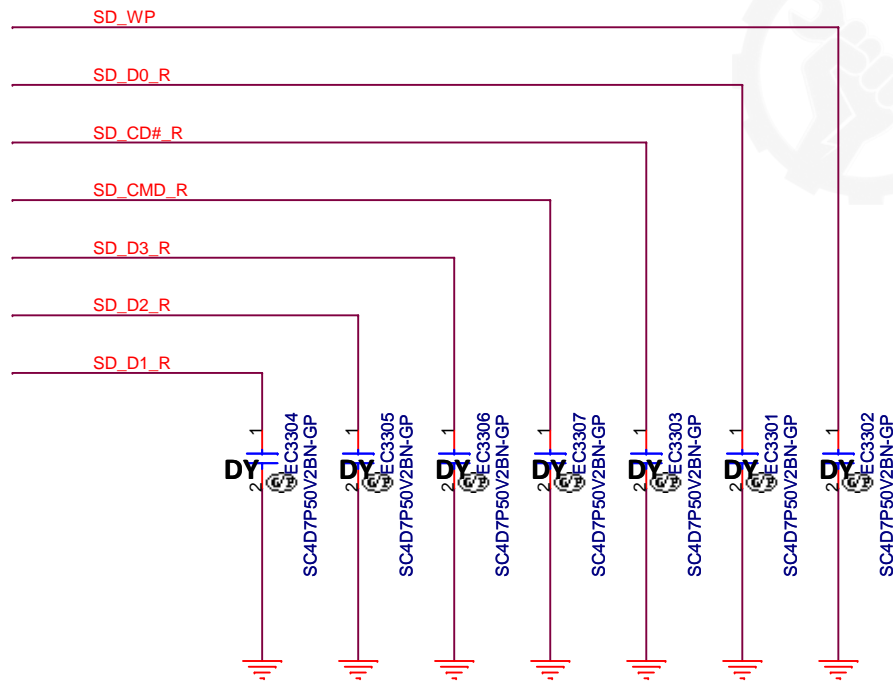




**Main Func = Card Reader**



**For EMI Reserved**



Without card	<p>CD is connected to GND through a resistor. WP is connected to GND through a resistor.</p>
Inserted card(lock)	<p>CD and WP are connected to a common node. This node is connected to GND through a resistor.</p>
Inserted card(unlock)	<p>CD and WP are connected to a common node. This node is connected to GND through a resistor. Additionally, there is a direct connection from the common node to GND.</p>

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### **Card Reader CONN**

Size  
A4

Document Number
-----------------

## Iris BTM

Rev

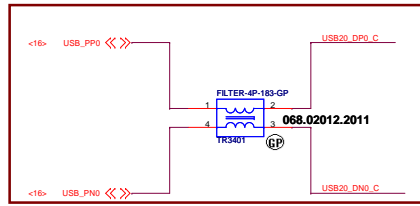
# A00

Date: Monday, November 17, 2014

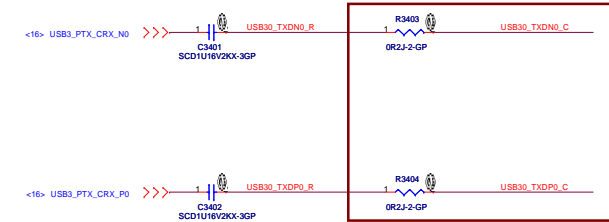
Sheet 33 of 102

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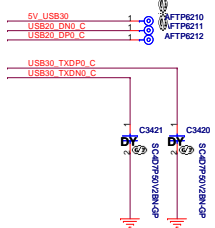
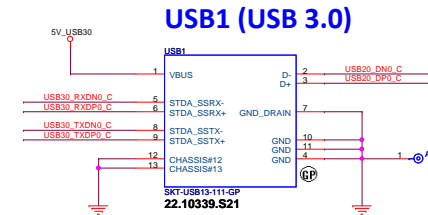
## Main Func = USB3.0 Port1



X02 change



X02 change



USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+

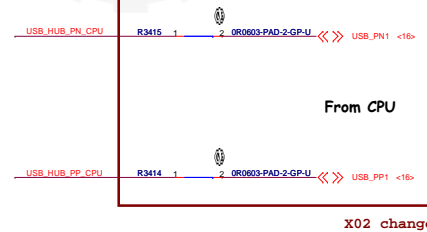
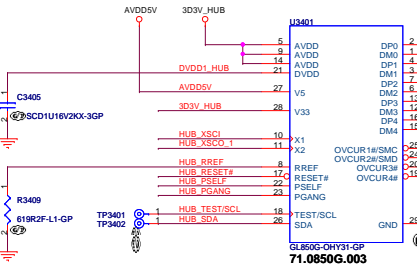
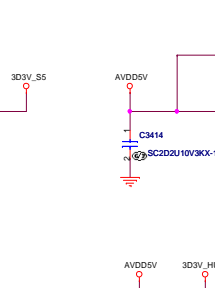
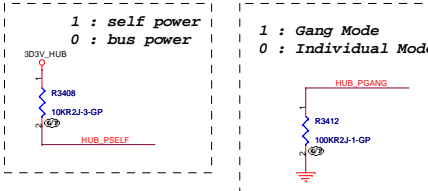
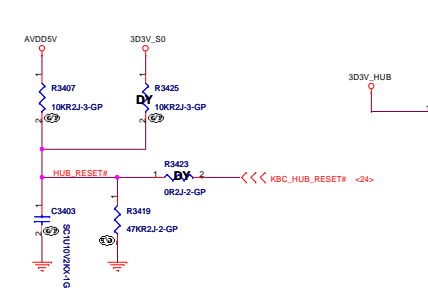
## Main Func = USB2.0 Port2

USB connector on I/O Board.

## Main Func = USB2.0 Port3

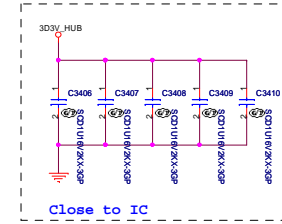
USB connector on I/O Board.

## Main Func = USB Hub

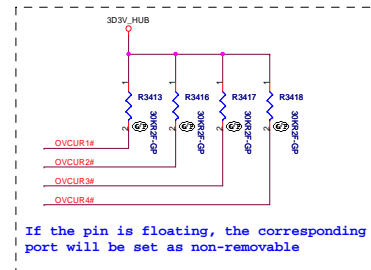


From CPU

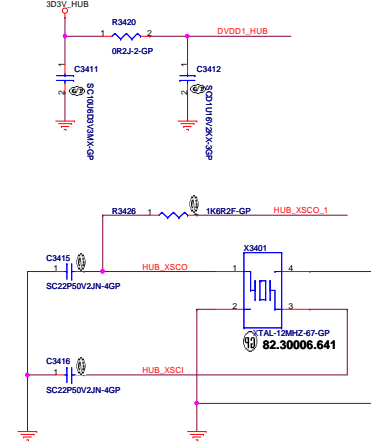
X02 change



Close to IC

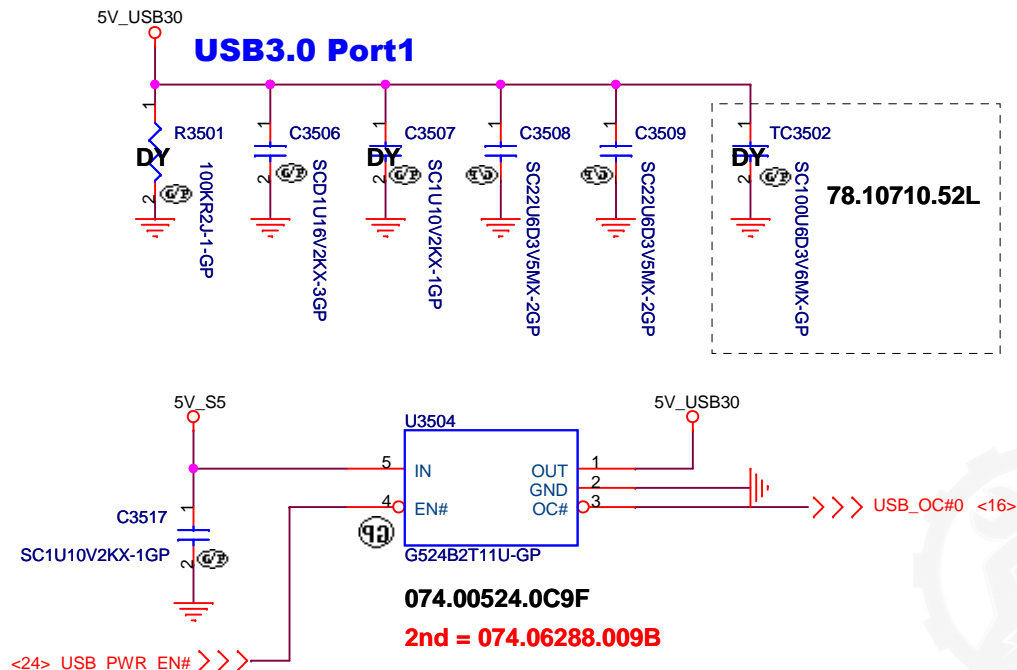


If the pin is floating, the corresponding port will be set as non-removable

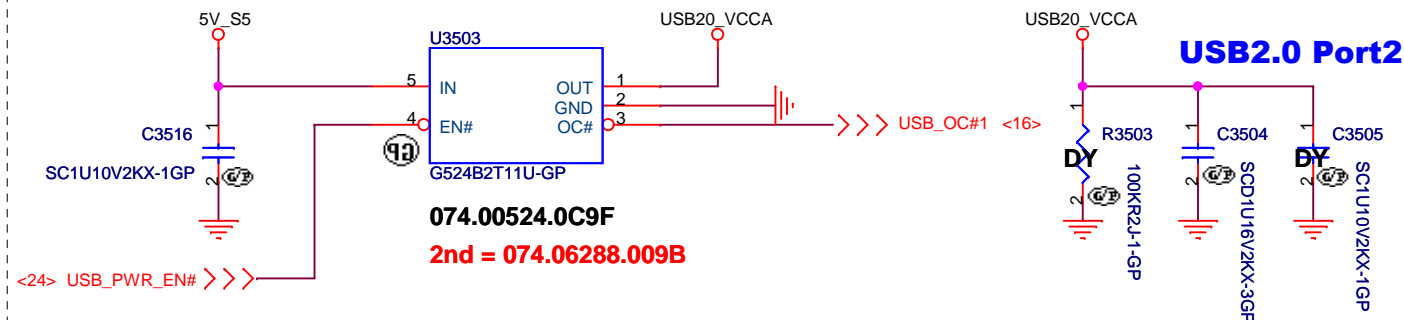


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## Main Func = USB3.0

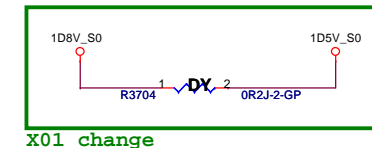
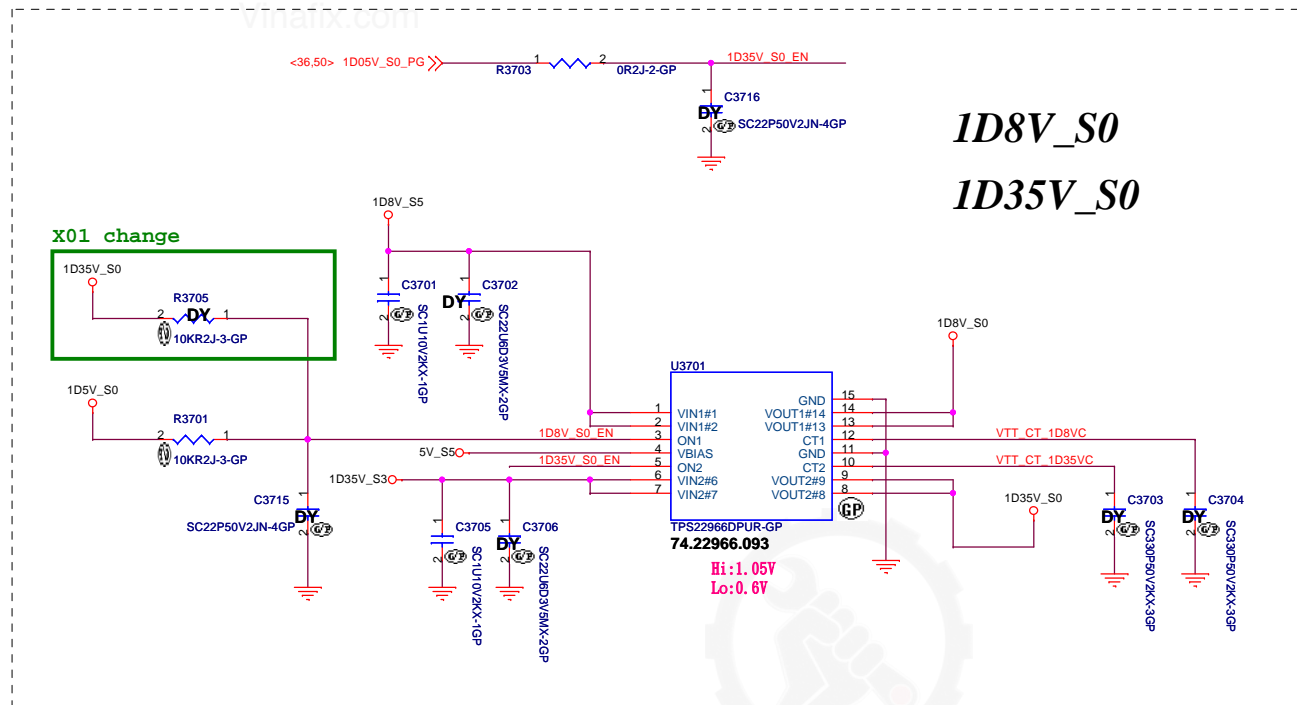


## Main Func = USB2.0

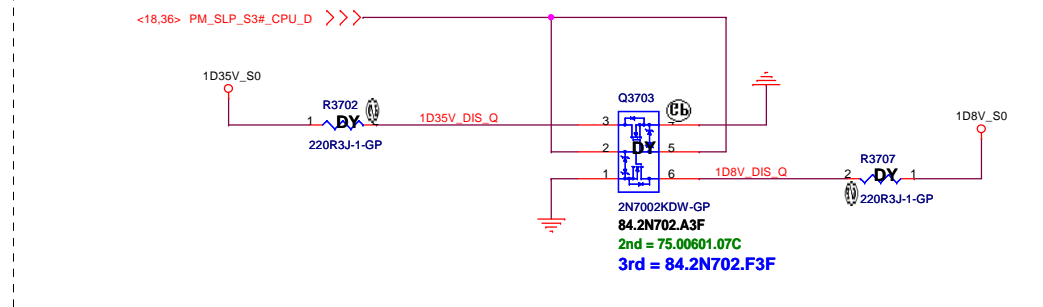




# Main Func = Power Plane & Sequence



## Discharge circuit




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Title				
Run Power				
Size	Document Number			Rev
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Date: Tuesday, November 11, 2014		Sheet 38	of 102


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Date: Tuesday, November 11, 2014		Sheet 39 of	102

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Size A4	Document Number <b>Iris BTM</b>		Rev <b>A00</b>
Date: Tuesday, November 11, 2014		Sheet 41	of 102

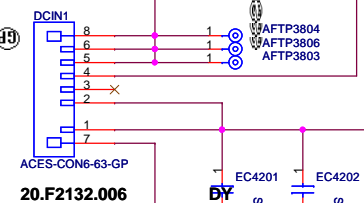
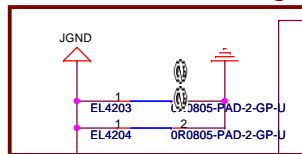
# Main Func = ADT Input

Vinafix.com

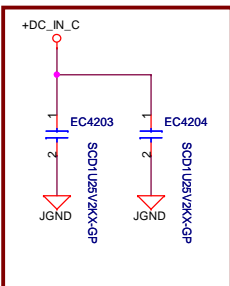
## Layout Note:

PSID Layout width > 25mil

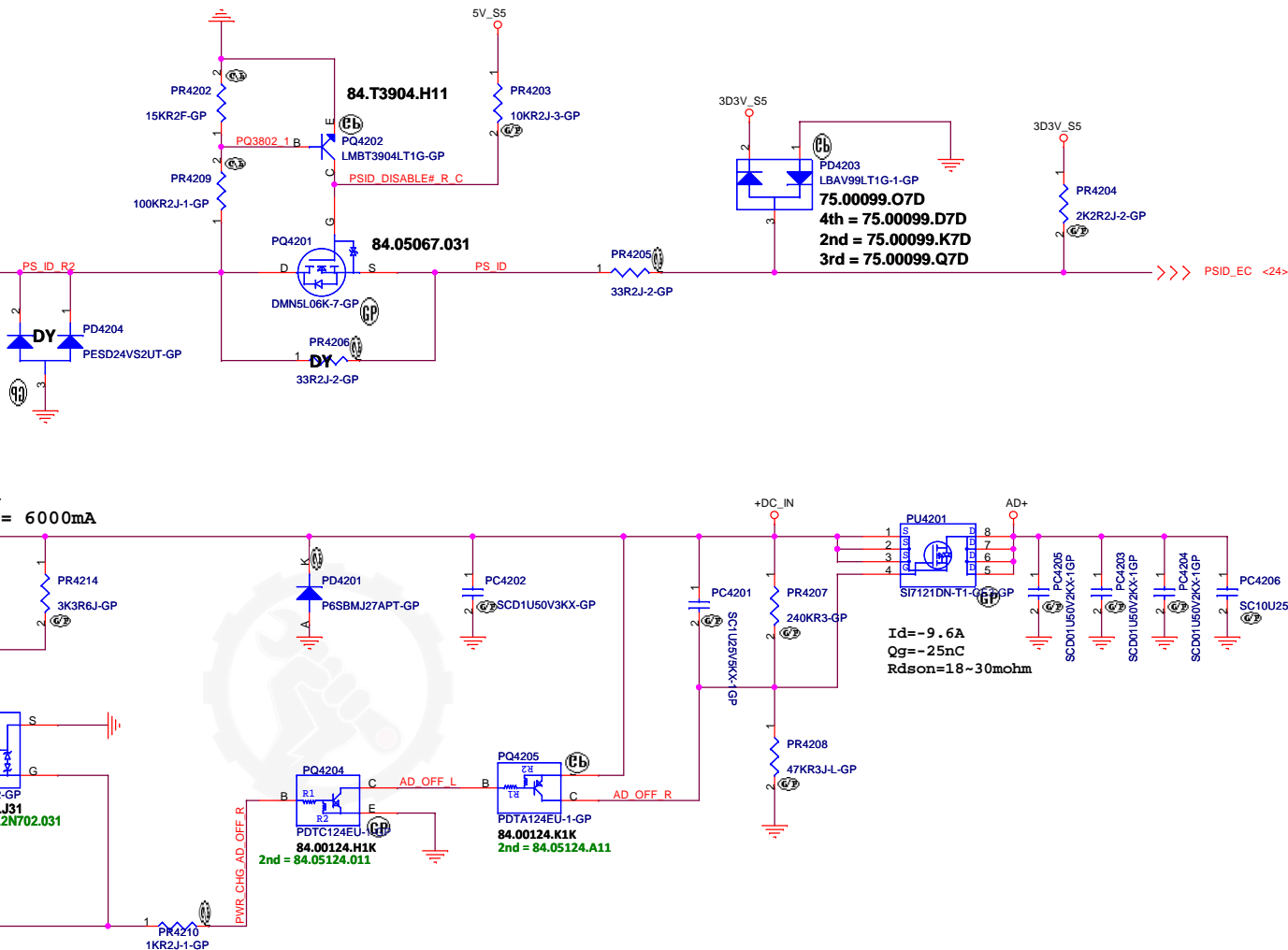
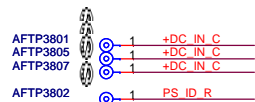
X02 change



60ohm@100MHz  
DCR=0.02 ohm  
Max current = 6000mA



X02 change

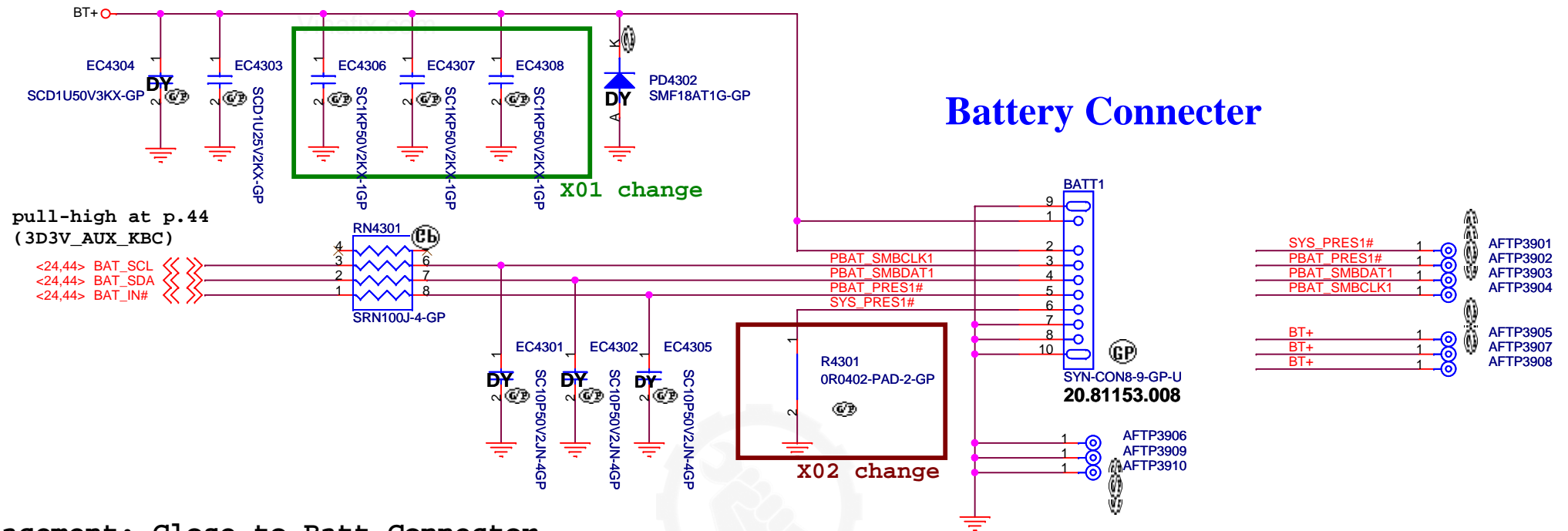


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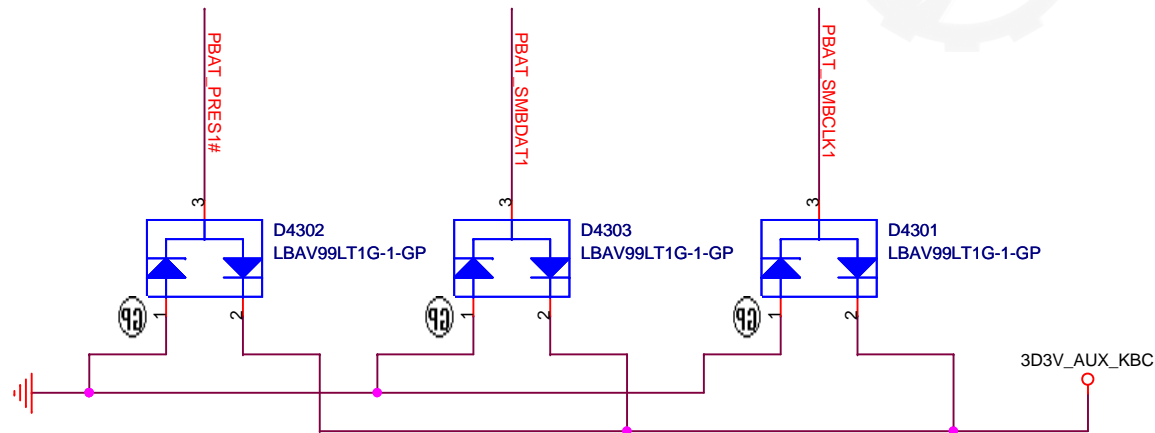
**DELL** Wistron Corporation  
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Title <b>DCIN JACK</b>		
Size A3	Document Number <b>Iris BTM</b>	Rev <b>A00</b>
Date: Monday, November 17, 2014	Sheet 42 of 102	

# Main Func = M-BAT Input



Placement: Close to Batt Connector



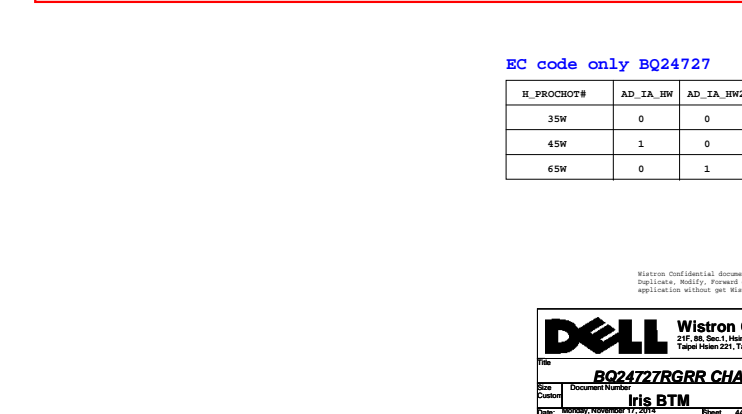
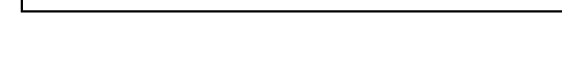
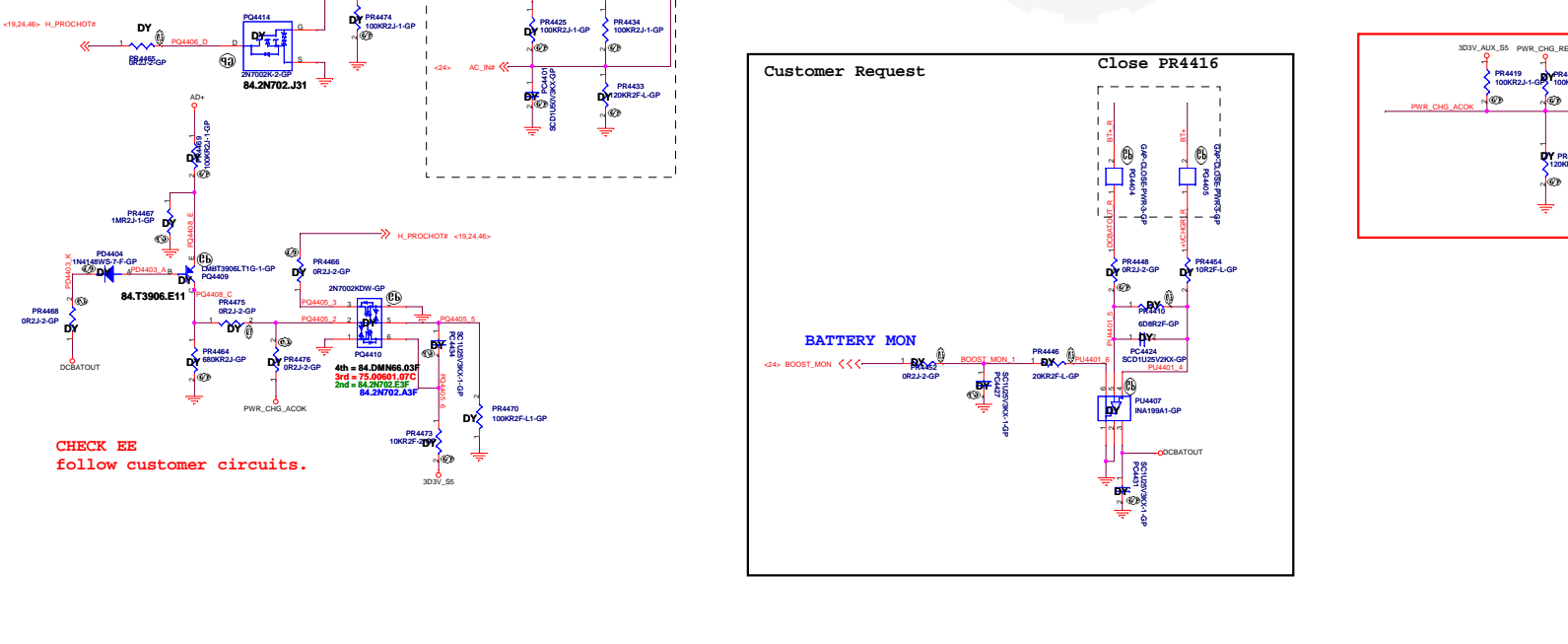
75.00099.07D  
2nd = 75.00099.K7D  
3rd = 75.00099.Q7D  
4th = 75.00099.D7D

75.00099.07D  
2nd = 75.00099.K7D  
3rd = 75.00099.Q7D  
4th = 75.00099.D7D

75.00099.07D  
2nd = 75.00099.K7D  
3rd = 75.00099.Q7D  
4th = 75.00099.D7D

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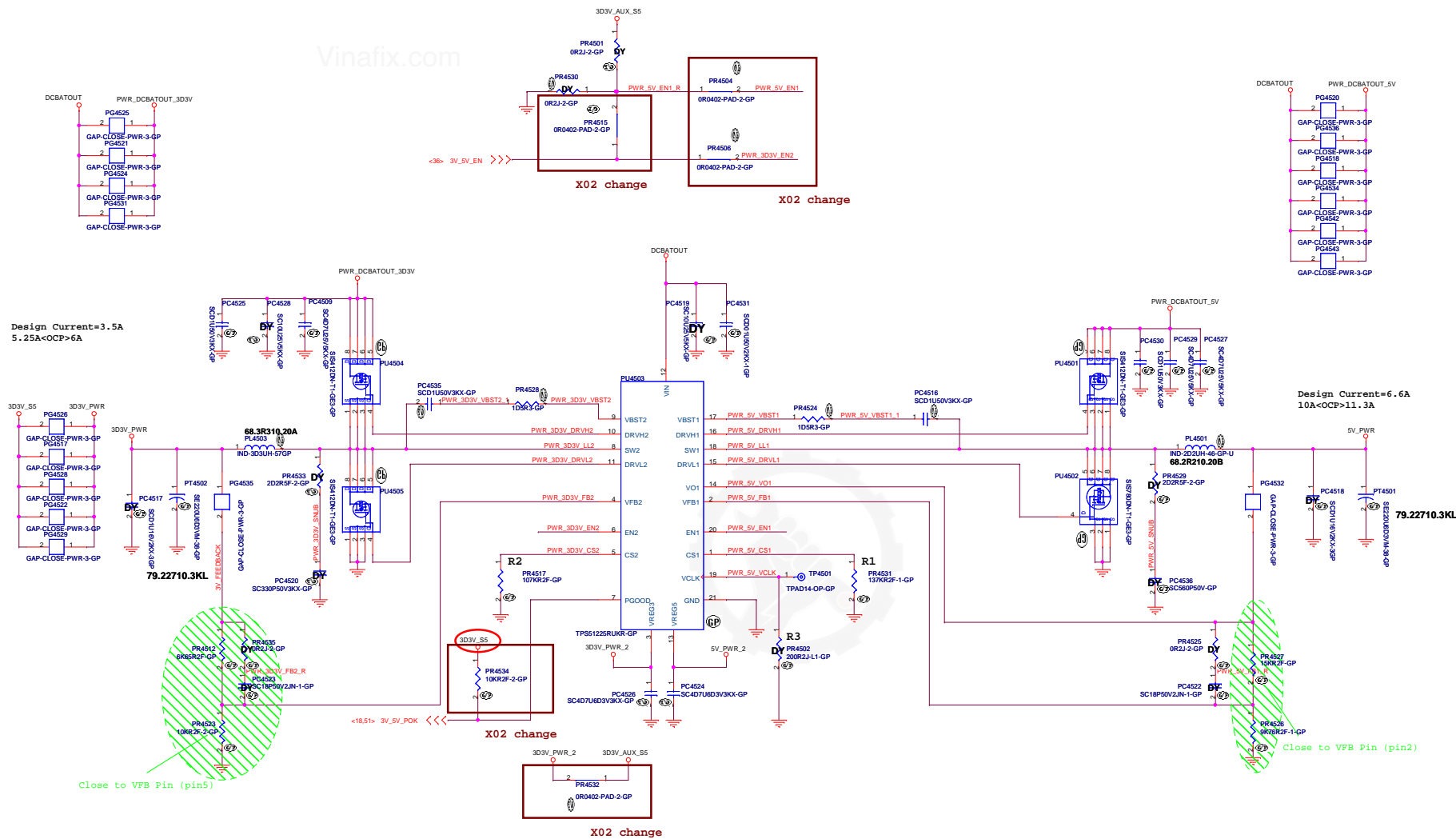
<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>BATT CONN</b>			
Size A4	Document Number <b>Iris BTM</b>		Rev <b>A00</b>
Date: Monday, November 17, 2014	Sheet 43	of	102



A photograph of a document. At the top, there is a large, stylized 'DELL' logo. Below the logo, the word 'Wistron' is printed in a bold, sans-serif font. Underneath 'Wistron', there is a line of text: '2UF, 88, Sec. 1, Hsin Taipei Hsien 221, T. R.'. Below this, there is a table with two columns: 'Serial Number' and 'Document Number'. The first row of the table contains the values 'BQ24727RGRR' and 'CHAI'. Below the table, the text 'Iris BTM' is printed in a large, bold, sans-serif font. At the bottom of the document, there is a line of text: 'MOORE, ROBERTA L. 1982'. The document is placed on a light-colored surface.

Main Func = 3D3V\_5V

Vinafix.com

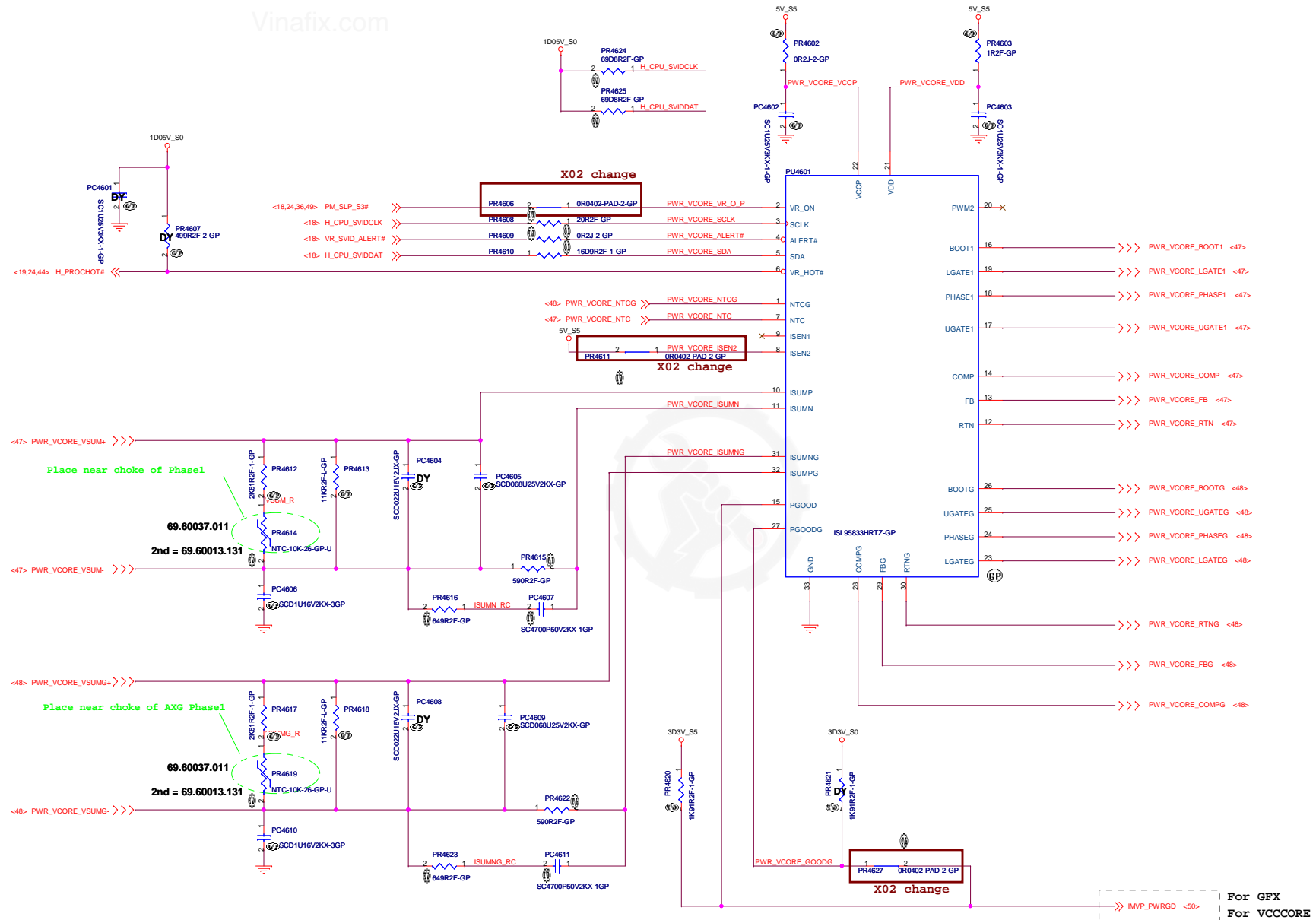


I/P cap: CHIP CAP C 10U 25V K0805 X5R / 78.10622.51L  
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A  
O/P cap: CHIP CAP EL 220U 6.3V M6 3+4.4 /Chemt-con / 18mohm / 79.22710.3KL  
H/S: SIS412 / 24mohm/30mohm@4.5Vgs / 84.00412.037  
L/S: SIS412 / 24mohm/30mohm@4.5Vgs / 84.00412.037

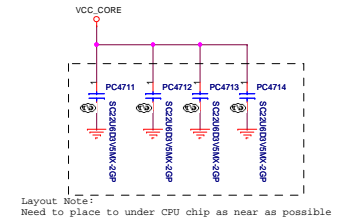
I/P cap: CHIP CAP C 10U 25V K0805 X5R / 78.10622.51L  
Inductor: CHIP CHOK 2.2U PCMC063T-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B  
O/P cap: CHIP CAP EL 220U 6.3V M6 3+4.4 /Chemt-con / 18mohm / 79.22710.3KL  
H/S: SIS412 / 24mohm/30mohm@4.5Vgs / 84.00412.037  
L/S: SIS780 / 14.5mohm/17.5mohm@4.5Vgs / 84.00780.037

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**Main Func = CPU\_CORE**



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Title _____			
<b>ISL95833 CPUCORE(2/3)</b>			
<b>Iris BTM</b>		<b>Rev A00</b>	
Date: Monday, November 17, 2014	Sheet 47	of	102

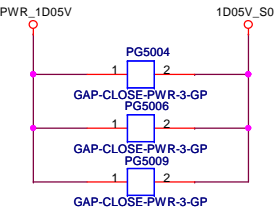
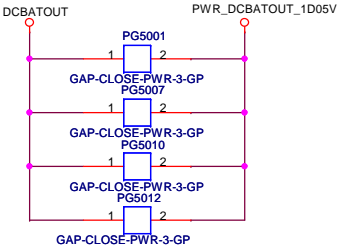






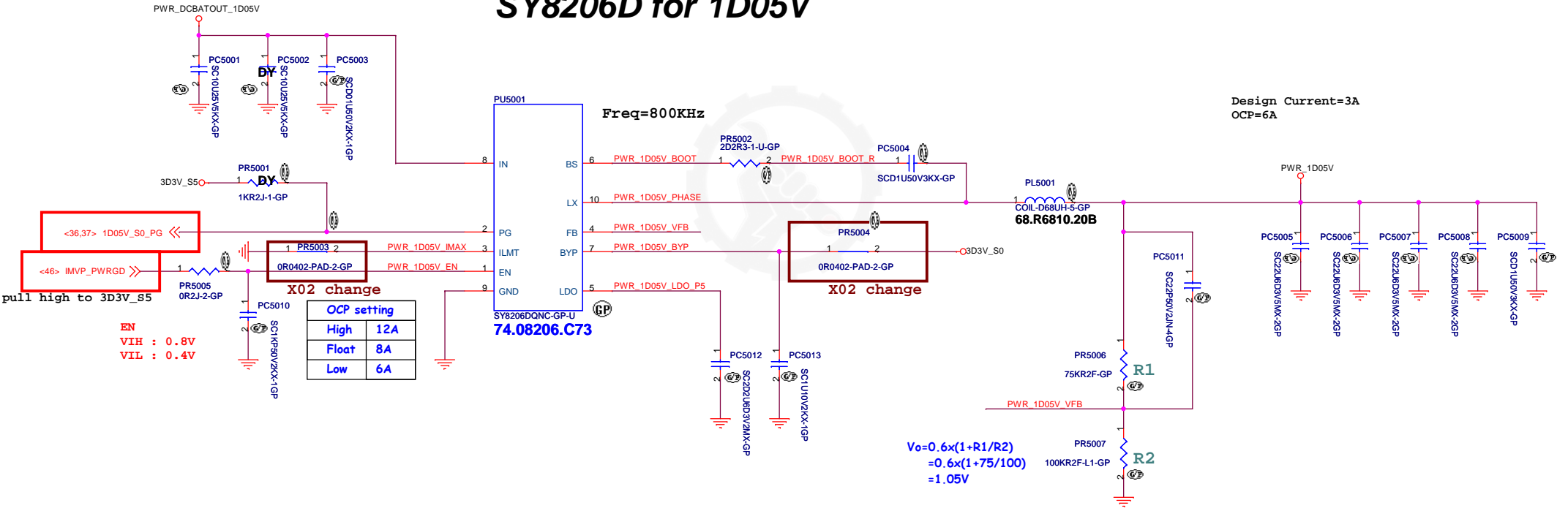
Main Func = 1D05V

Vinafix.com



# SY8206D for 1D05V

Design Current=3A  
OCP=6A

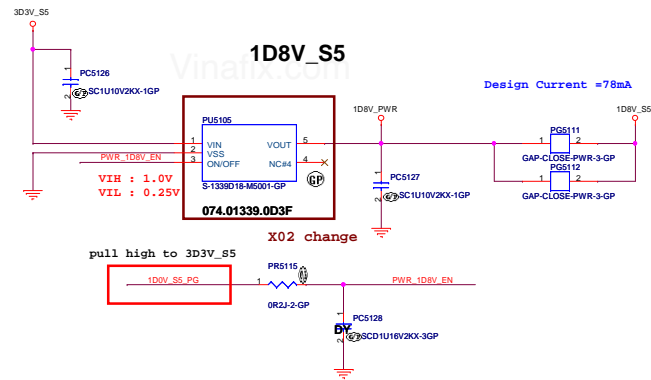


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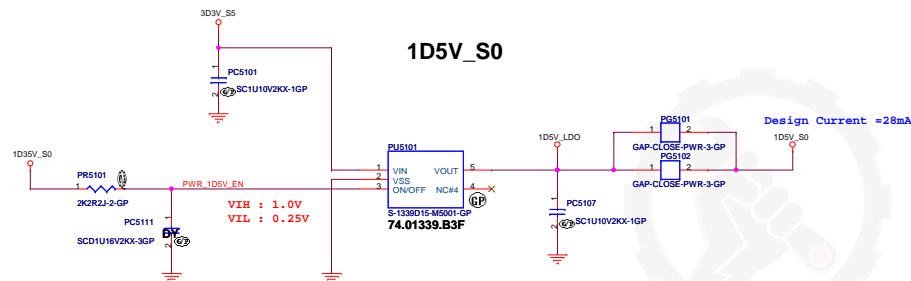
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Title			SY8206D DCDC 1D05V	
Size			Document Number	
A3			Iris BTM	
Date:			Monday, November 17, 2014	Sheet 50 of 102
			Rev	A00

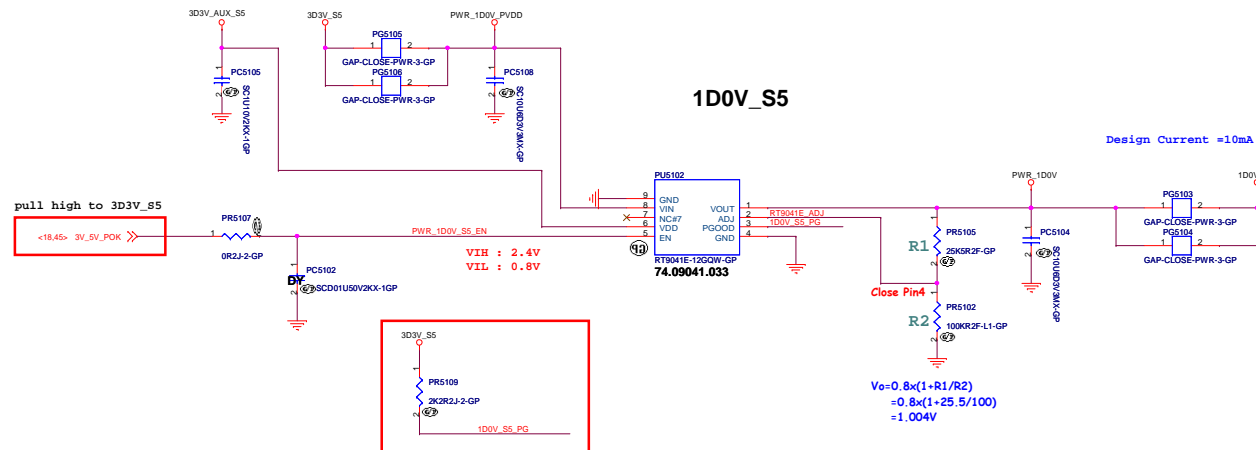
Main Func = 1D8V



Main Func = 1D5V



Main Func = 1D0V




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# Blanking

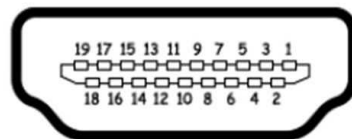
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Title			
<b>Reserved</b>			
Size A4	Document Number <b>Iris BTM</b>		Rev <b>A00</b>
Date: Tuesday, November 11, 2014		Sheet 53	of 102

Main Func = HDMI

# HDMI Level Shifter & Connector

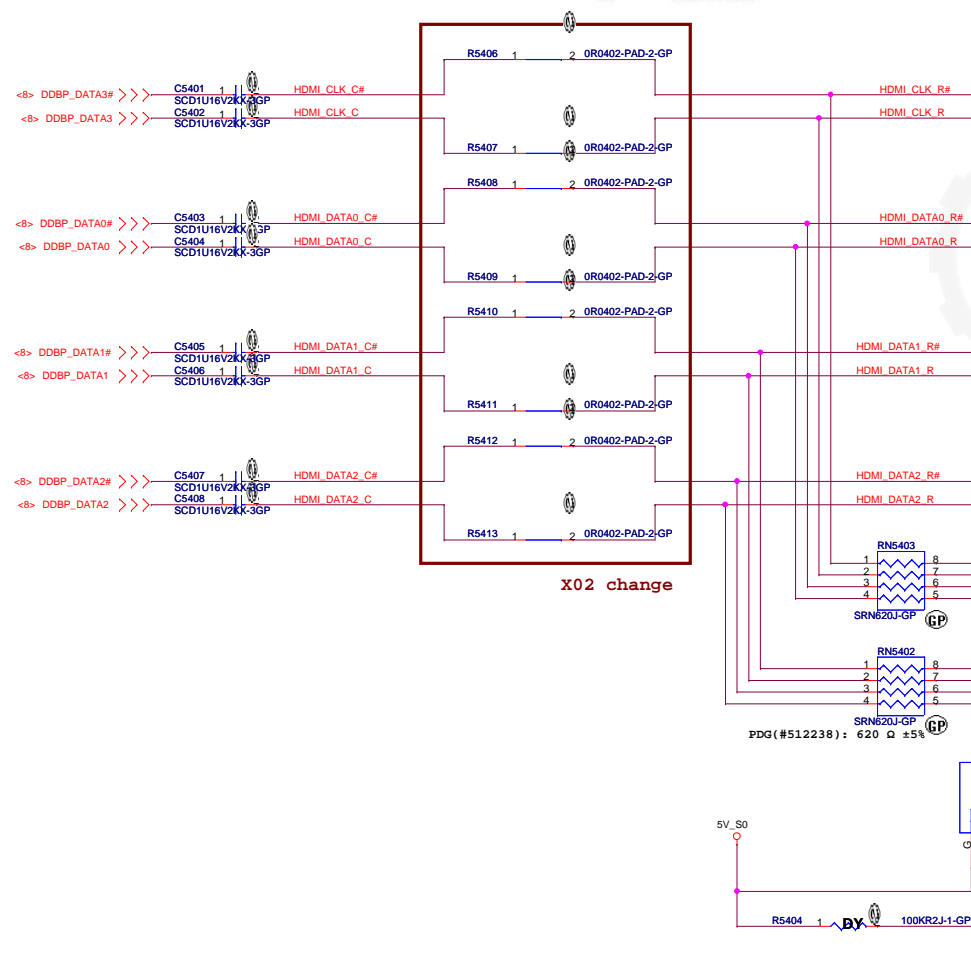
Vinafix.v



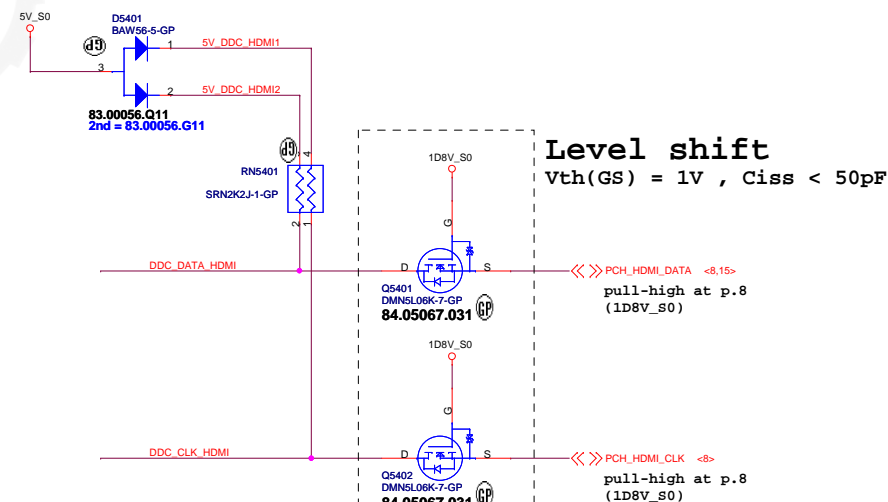
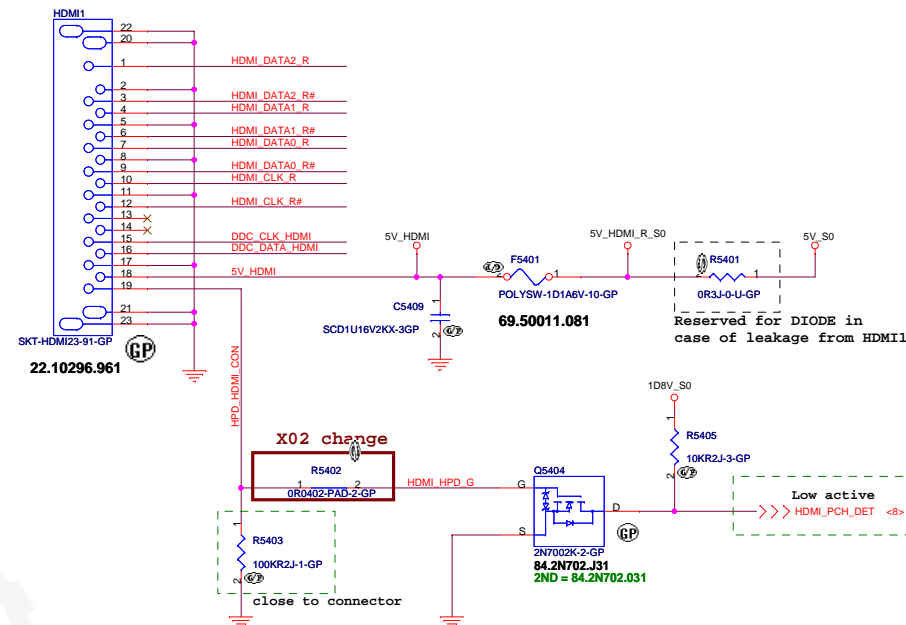
HDMI\_CLK\_R# R5414 1 150R2F-1-GP HDMI\_CLK\_R  
HDMI\_DATA0\_R# R5415 1 150R2F-1-GP HDMI\_DATA0\_R  
HDMI\_DATA1\_R# R5416 1 150R2F-1-GP HDMI\_DATA1\_R  
HDMI\_DATA2\_R# R5417 1 150R2F-1-GP HDMI\_DATA2\_R

Reserve 150 ohm bridge resistance on the HDMI trace as circle for EMI.

Pin#	Signal	Pin#	Signal
1	TMDS data 2+	11	TMDS clock shield
2	TMDS data 2 shield	12	TMDS clock-
3	TMDS data 2-	13	CEC
4	TMDS data 1+	14	No connected
5	TMDS data 1 shield	15	DDC clock
6	TMDS data 1-	16	DDC data
7	TMDS data 0+	17	Ground
8	TMDS data 0 shield	18	+5V power
9	TMDS data 0-	19	Hot plug detect
10	TMDS clock+		




## HDMI Connector



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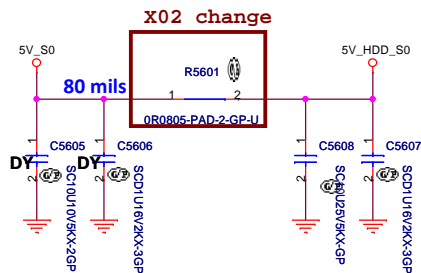
# Blanking

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b><i>Reserved</i></b>			
Size A4	Document Number <b>Iris BTM</b>		Rev <b>A00</b>
Date: Tuesday, November 11, 2014		Sheet 55	of 102

Main Func = HDD

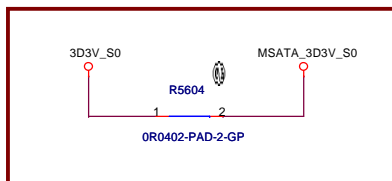
Vinafix.com

## SATA HDD Connector

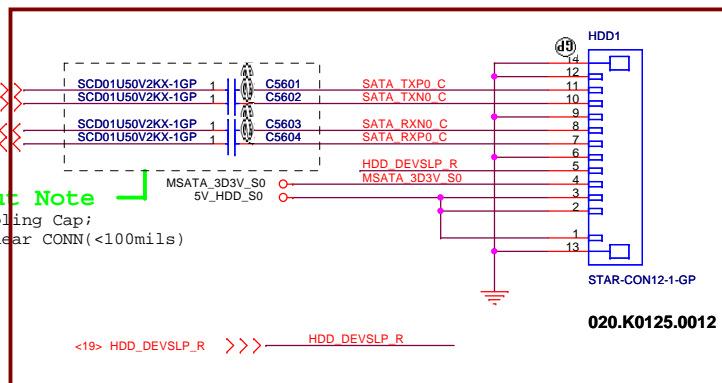


<19> SATA0\_PTX\_DRX\_P0  
<19> SATA0\_PTX\_DRX\_N0  
<19> SATA0\_PRX\_DTX\_N0  
<19> SATA0\_PRX\_DTX\_P0

**Layout Note**  
AC coupling Cap;  
place near CONN(<100mils)

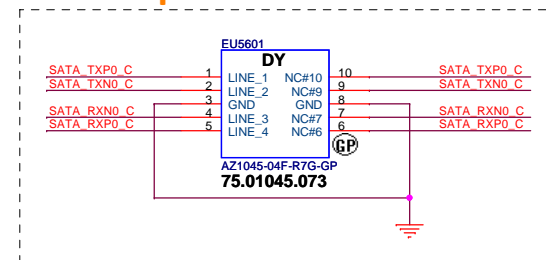


**X02 change**



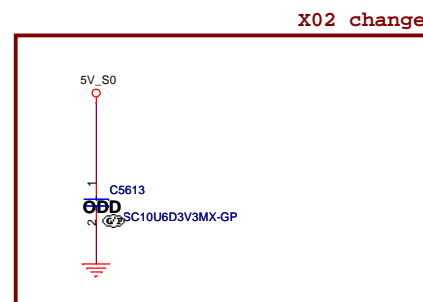
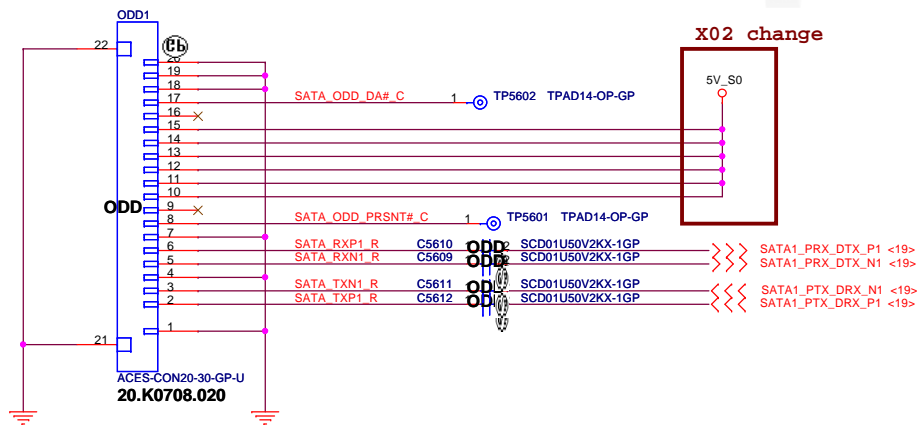
**X02 change**

## EMI Request



Main Func = ODD

## ODD Connector



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Title			HDD/ODD	
Size	Document Number	Rev		A00
A3	Iris BTM			
Date:	Monday, November 17, 2014	Sheet	56	of 102



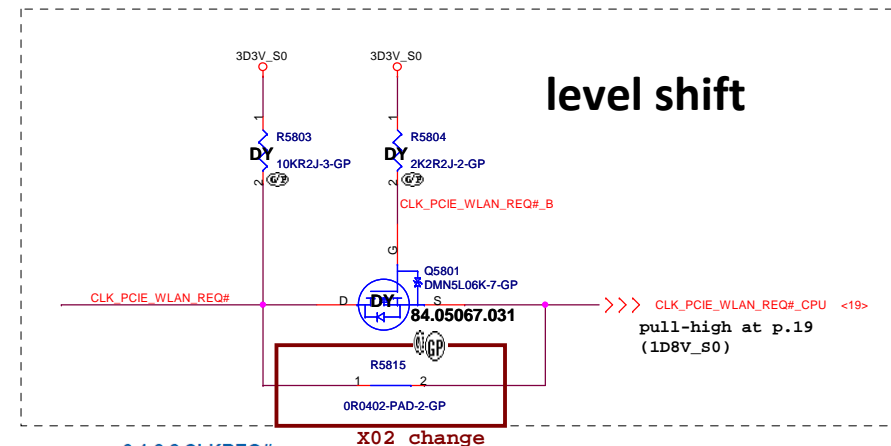
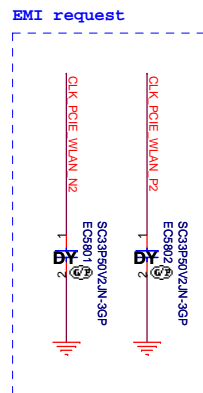
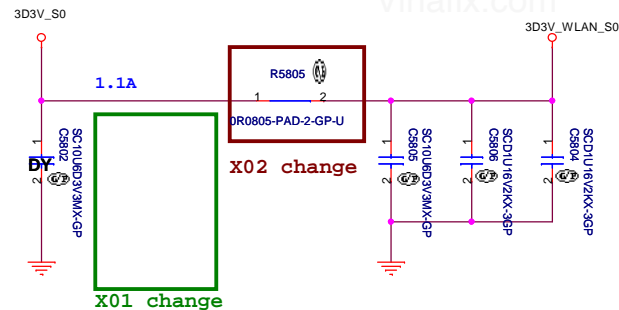
(Blanking)



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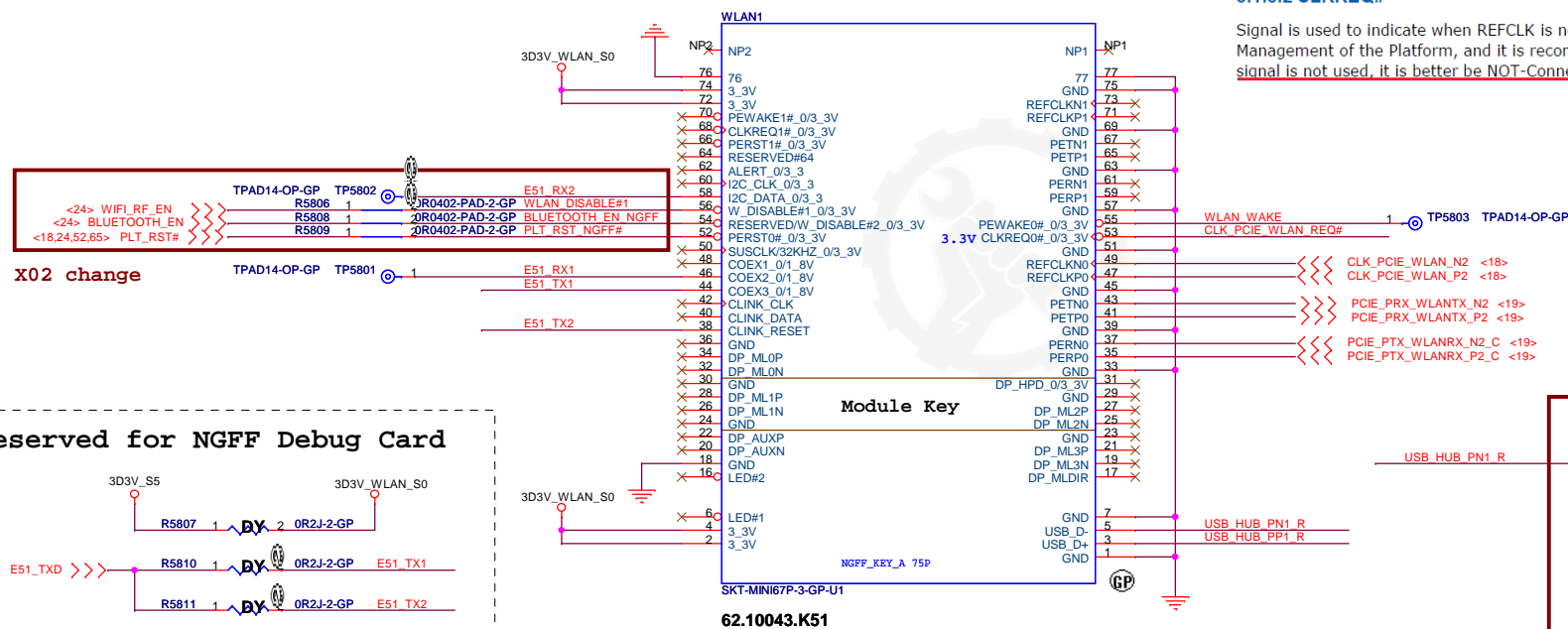
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)</b>			
Size A4	Document Number <b>Iris BTM</b>		Rev <b>A00</b>
Date: Tuesday, November 11, 2014		Sheet 57 of	102

**Main Func = WLAN**

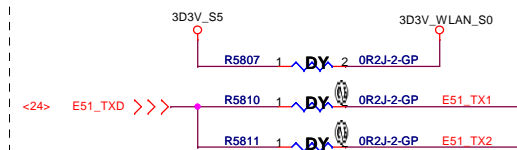


### 3.1.8.2 CLKREQ#

Signal is used to indicate when REFCLK is needed, this is usually needed for advanced Power Management of the Platform, and it is recommended but not a mandatory (optional) Signal. If the signal is not used, it is better be NOT-Connected in the Platform board level.

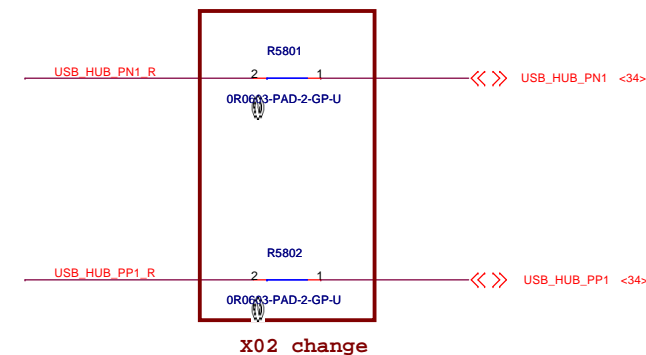


Reserved for NGFF Debug Card



EE Note:  
For NFGG Debug Card:  
Stuff R5807,R5810,R5811(optional).  
DY R5805.

AFTP5801	1	3D3V WLAN S0
AFTP5802	1	CLK PCIE WLAN REQ#
AFTP5803	1	WLAN DISABLE#1
AFTP5804	1	BLUETOOTH_EN NGFF
AFTP5805	1	PLT_RST NGFF#
AFTP5806	1	USB HUB PN1 R
AFTP5807	1	USB HUB PP1 R



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Main Func = WWAN/mSATA

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Title <b>(Reserved)</b>			
Size A4	Document Number <b>Iris BTM</b>		Rev <b>A00</b>
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Main Func = mSATA

Vinafix.com

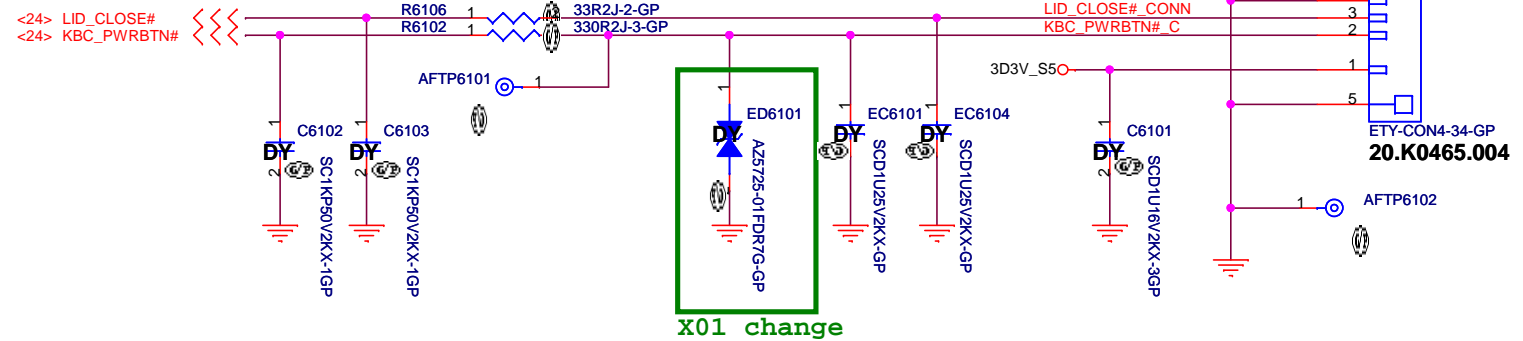
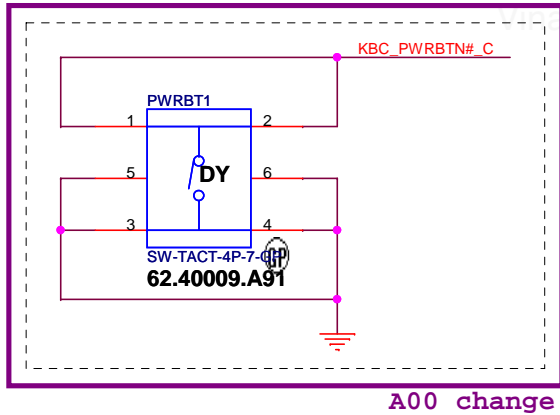
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Title <b>(Reserved)</b>			
Size A4	Document Number <b>Iris BTM</b>		Rev <b>A00</b>
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## Main Func = Power BTN

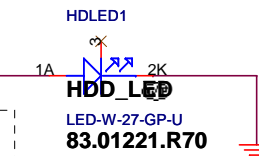
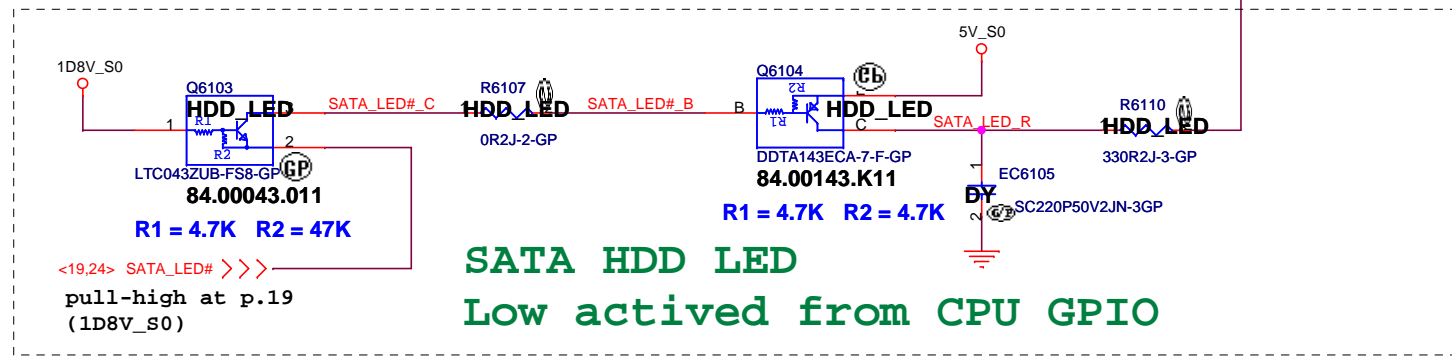
## Power Button & Hall Sensor



## Main Func = LED

Battery LED1  
Low activated from KBC GPIO

Battery LED2  
Low activated from KBC GPIO



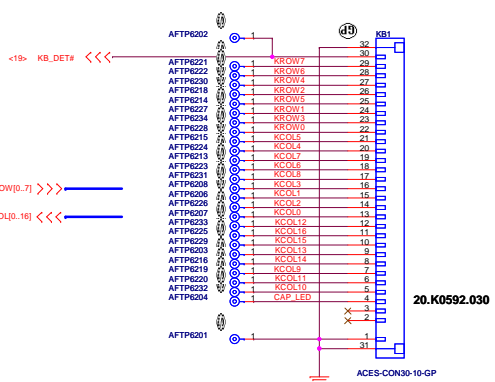
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: <b>LEDBard/PowerButton</b>			
Size Custom	Document Number	Rev A00	
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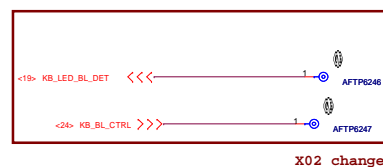
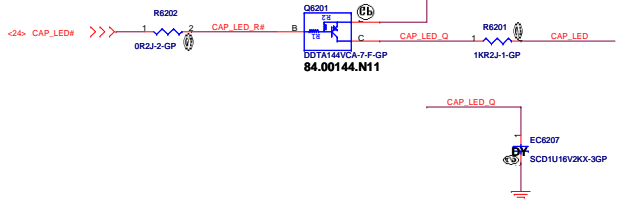
Main Func = KB

## Keyboard

### Internal Keyboard Connector (14")

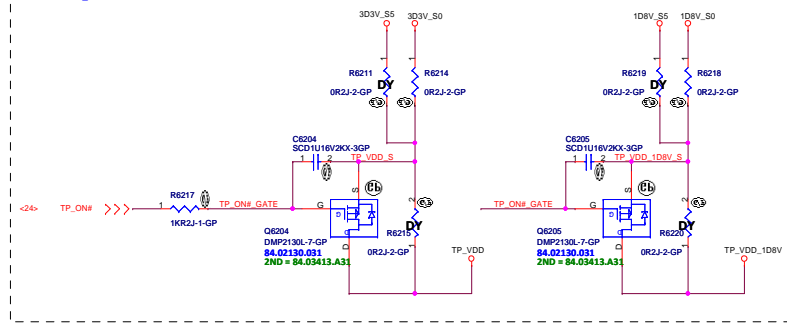


### CAP LED Control LOW active from KBC GPIO

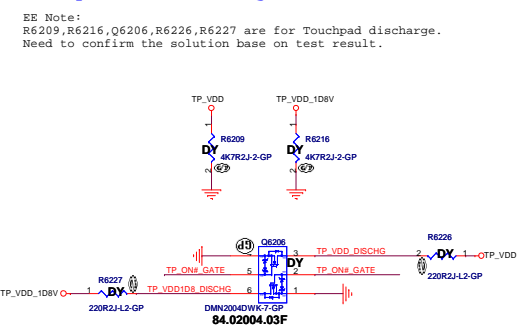


Main Func = TPAD

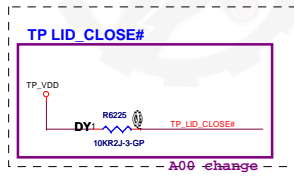
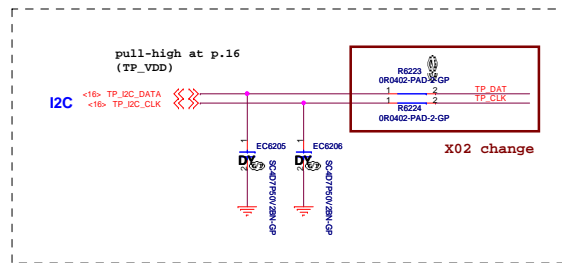
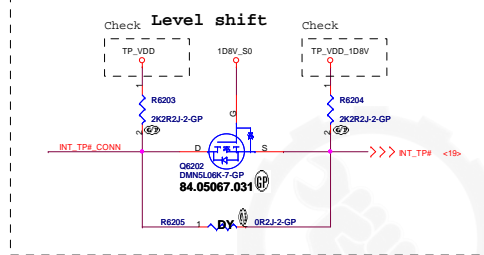
### Touchpad Power



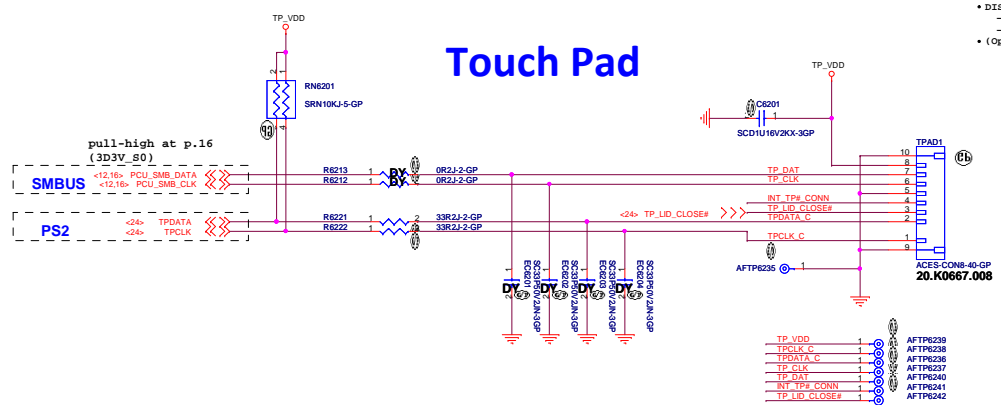
### Touchpad Power Discharge



### INT#



## Touch Pad

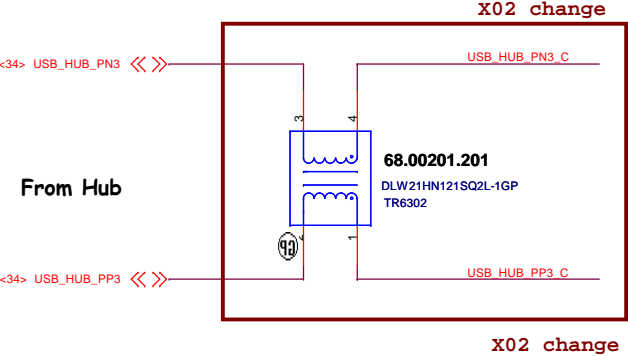
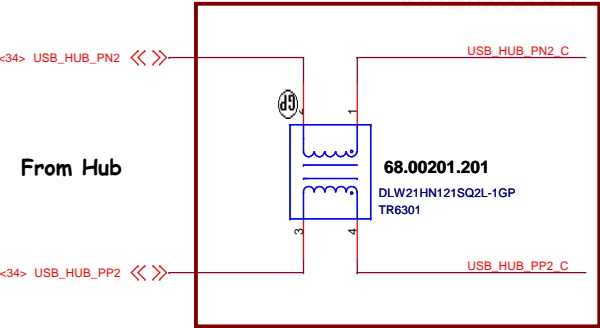


(#514849) I2C PTP Pins  
Standard I2C pins for interrupt driven I2C device:  
• +3.3V VDD  
• GND  
• SCL (clock)  
• SDA (data)  
• INT# (or INTR#, interrupt), also known as ATTN# (attention)  
-Active low  
Other pins needed on I2C PTP:  
• wake# - level trigger signal from PTP to Host  
-Overload the INTR#/ATTN# line (on the same pin)  
-Only used during S3  
-Active low  
-Connect to either wake capable mechanism on chipset  
• GPIO pin (suspend Well powered) for S3 platform  
• GPIO on EC (and route to GPIO27 or PWRBTN# on chipset)  
• DSW (interrupt disable)  
-level trigger signal from sensor (slate mode decider) to PTP  
-Active low (active = disable any interrupt, including wake)  
• (Optional) +1.8V VDD

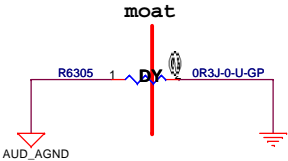
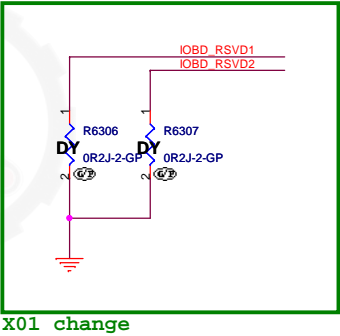
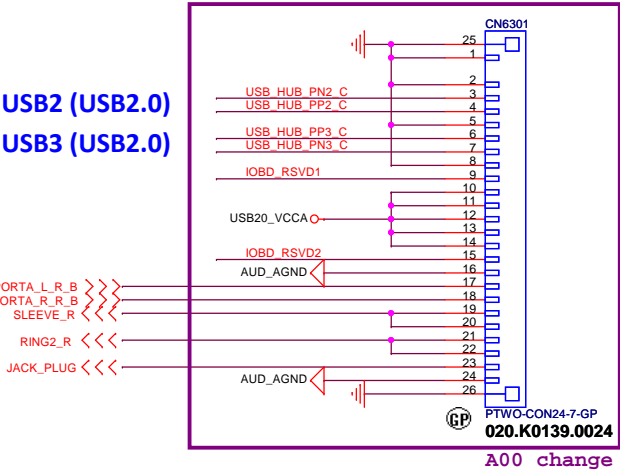
Pin No.	Pin name
1	VDD (3.3V)
2	DAT (I2C)
3	CLK (I2C)
4	GND
5	INT#
6	GPIO
7	DAT (PS2)
8	CLK (PS2)

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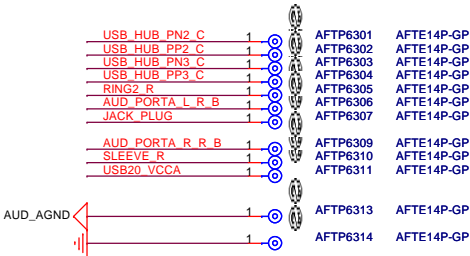
Main Func = IO Connector



# I/O Board Connector



Pitch: 1mm  
Power: 5 pins  
GND: 4 pins  
AGND: 2 Pins



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IO Board Connector		
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Main Func = Hall Sensor

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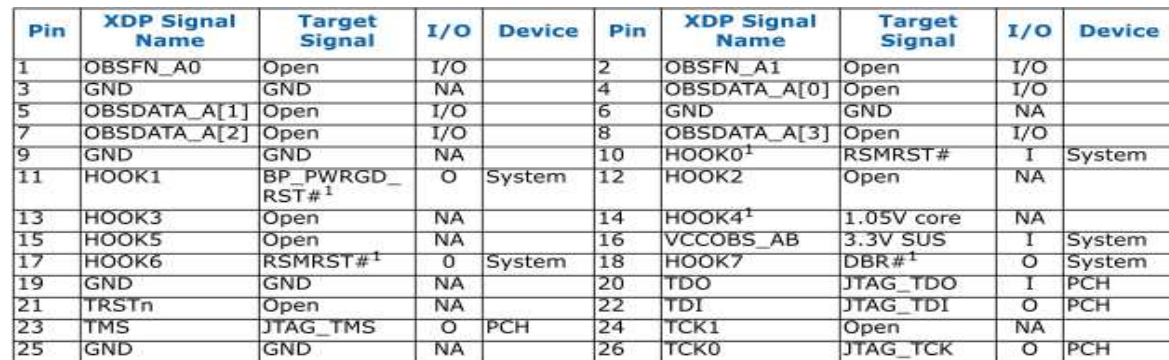
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<b><i>Debug connector</i></b>			
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Main Func = Sensor Hub+Accelerometer (G-Sensor)+Gyro+Proximity SAR+ALS

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Main Func = G-Sensor

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Main Func = Thunderbolt

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Main Func = dGPU

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Main Func = dGPU

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5 4 3 2 1


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Main Func = dGFX\_CORE

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Main Func = dGPU

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Main Func = GFXLCD

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Main Func = GFXCRT

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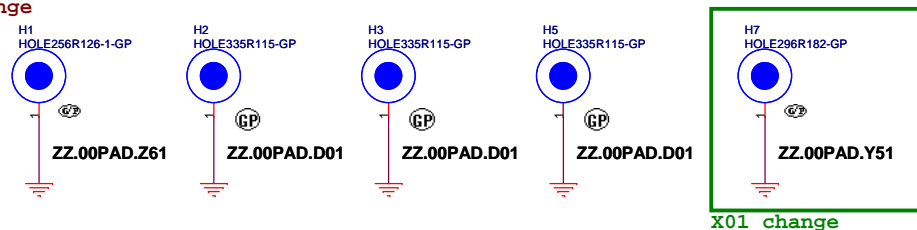
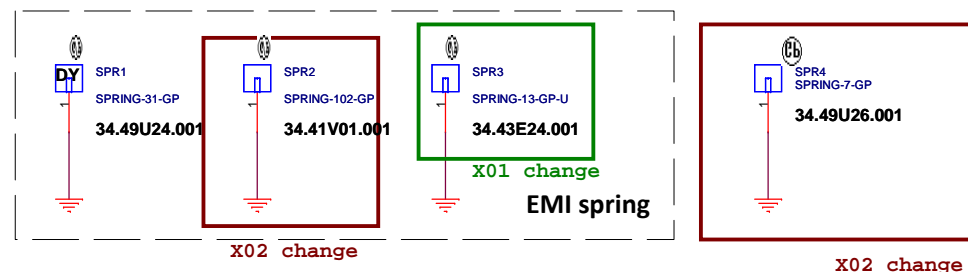
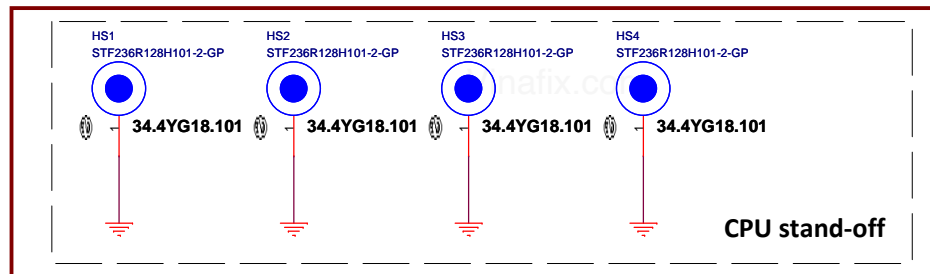
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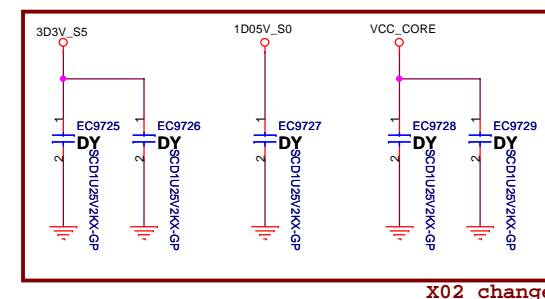
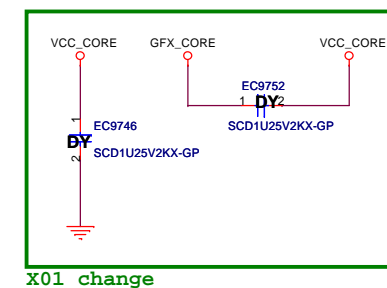
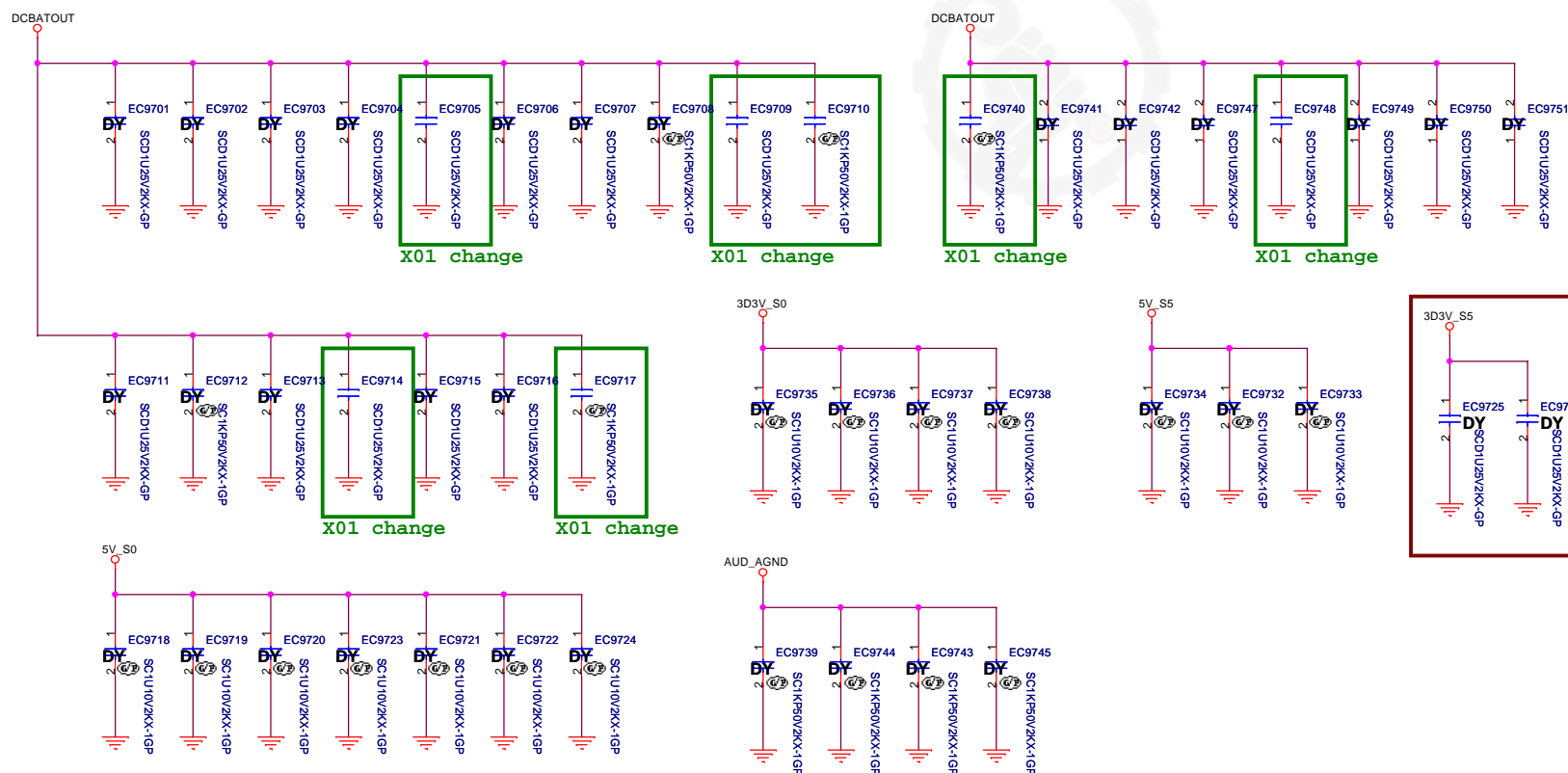
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**Main Func = Unused Parts**



## Main Func = EMI Capacitors




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Main Func = NFC

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Main Func = TPM

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Main Func = FPR

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Main Func = SmartCard

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Main Func = SmartCard

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Main Func = Switchable

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Main Func = Dock

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Main Func = LAN

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Main Func = LAN

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Main Func = Debug

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Change History

Ver.	Date	Page	Change Description	Reasons
X00	06/18	18	Change C1806, C1807 to 7pF	CPU 32K Xtal fix. (X1802)
X00	06/18	34	Change C3415, C3416 to 22pF, add R3426.	USB hub 12M Xtal fix. (X3401)
X01	08/12	86	Add H7.	Dell ME and UI request.
X00	06/18	35	Mount R3502, R3505, dummy U3505, C3518.	No layout space for adding H7.
X00	06/18	51	Change PU5102.6 to 3D3V_AUX_S5.	Fix power down sequence. (1D0V_S5_PG)
X00	07/01	24,62	Mount R2408 and R6225.	Touchpad lid close function.
X00	07/01	24,26	Mount R2468 and R2603, dummy R2601.	Use KBC T8.
X01	07/31	24	Add R2438.	SATA LED indicate.
X01	07/31	37	Reserve R3704, R3705.	Reserve 1.5V bypass to 1.8V.
X01	07/31	52	Reserve ED5201.	ESD protection for MP.
X01	07/31	56	Add R5604.	mSATA power.
X01	07/31	63	Reserve R6306, R6307.	ESD protection for CM mode.
X01	08/04	54	Reserve TR5401~TR5404.	EMI for CM mode.
X01	08/11	58	Delete C5801, C5803.	No layout space for adding H7.
X01	08/11	61	Reserve ED6101.	EMI for power BTN.
X01	08/11	86	Reserve EC9746, EC9752.	EMI for CM mode.
X01	08/12	29	Mount EC2901~EC2904	EMI request for speaker noise.
X01	08/12	43	Add EC4306~EC4308.	EMI request for BT+ power noise.
X01	08/12	86	Mount EC9705, EC9709, EC710, EC9714, EC9717, EC9740, EC9748 and SPR3.	EMI request for DCBATOUT power noise.
X01	08/14	24	Reserve Q2405, R2470.	SATA/WHITE LED switch.
X01	08/27	34, 52 ,63	Change TR3401, TR5203, TR6301, TR6302 to 068.02012.2011.	EMI request for USB noise.
X02	09/22	44	1. Change PR4413 to 169kohm. 2. Change PR4429 to 309kohm. 3. Change PR4427 to 78.7kohm.	Power team request for 35W power companion.
X02	09/26	24	change R2424 from 64.33025.6DL (33k) to 64.47025.6DL (47k)	PCB Version
X02	09/26	45	change PR4534 from 63.10434.1DL (100k) to 64.10025.6DL (10k)	Correct 3V_5V_POK 2.7V to 3.3V
X02	09/26	24	dummy R2438 ; stuff R2471,Q2405	For ROSA HDD LED Function
X02	09/26	86	HS1~HS4 change from 34.4Z003.201 to 34.4YG18.101	Use stand off without mylar
X02	09/26	19,56	add R1915, R1908, Q1901, CPU1.BA24 (SATA_DEVSLEP_0) add HDD1.5(HDD_DEVSLEP_R)	DEVSLEP Function
X02	09/29	51	PU5105 change from 74.01339.D3F to 074.01339.0D3F	tape direction (power IC)
X02	09/29	56	HDD conntetor change from 020.K0016.0012 to 020.K0125.0012	change PTH type
X02	09/29	34,52 63	TR3401 ( 068.02012.2011 ) :SWAP TR5203 ( 068.02012.2011 ) :SWAP TR6301 ( 068.02012.2011 ) :SWAP TR6302 ( 068.02012.2011 ) :SWAP	CMC change from 68.00201.201 to 068.02012.2011
X02	10/01	19	del RN1903, CPU1.BB5 ; CPU1.BB7 change to connect GND	Layout space
X02	10/01	25	del SKT25	delete co-lay
X02	10/01	32	del TR3201	delete co-lay
X02	10/01	34	del R3401 R3402 ; TR3402, TR3403, TR3405	delete co-lay
X02	10/01	52	del R5223 R5224 ; TR5202	delete co-lay

Ver.	Date	Page	Change Description	Reasons
X02	10/01		RN2701 RN802 change from 66.R0036.04L to ZZ.0R04P.ZZZ	change to short pad
X02	10/01		R5601 R5805 change from 63.R0031.16L to ZZ.00PAD.M31	change to short pad
X02	10/01		RN6501 change from 66.R0036.A8L to ZZ.0R08P.ZHH	change to short pad
X02	10/01		R2706 R2906 R2907 R2909 R2911 R2405 R2703 R2704 R2711 R2901 R2902 R2903 R2904 R3201 R3202 R3414 R3415 R5801 R5802 change from 63.00000.00L to ZZ.00PAD.M21	change to short pad
X02	10/01		PR4422 PR4426 PR4504 PR4506 PR4515 PR4532 PR4627 R1203 R1207 R1210 R1211 R1827 R1832 R1836 R1924 R1925 R1928 R1929 R2102 R2104 R2408 R2410 R2414 R2416 R2427 R2429 R2430 R2434 R2453 R2460 R2461 R2507 R2509 R2510 R2511 R3302 R3303 R3304 R3305 R3306 R3619 R4301 R5201 R5210 R5402 R5806 R5808 R5809 R6223 R6224 R6507 R6508 R701 PR4606 PR4611 PR4712 PR4812 PR5003 PR5004 R1608 R1611R1614 R1615 R1616 R1818 R2415 R2419 R2422 R2441 R2449 R2465 R2467 R2610 R2613 R2701 R2702 R2705 R2708 R2714 R2716 R2720 R3205 R3301 R3403 R3404 R3405 R3406 R5406 R5407 R5408 R5409 R5410 R5411 R5412 R5413 R5604 R5815 change from 63.R0034.1DL to ZZ.00PAD.M11	change to short pad
X02	10/01	54	del TR5401 TR5402 TR5403 TR5404	delete co-lay
X02	10/01	42	EL4203 change to two ZZ.00PAD.M31	change to short pad
X02	10/01	52	stuff EC5201 EC5202	EMI DMIC noise
X02	10/01	86	stuff SPR2	EMI 1G noise
X02	10/02	56	del R5603 R5602, change net ODD_PWR_5V to 5V_S0	layout spacing
X02	10/02	62	remove KB_BL1 C6202 C6203 F6201 R6210 R6207 R6206 R6208 Q6203	Tulip feature matrix modify
X02	10/03	63	del TR6301 TR6302	delete co-lay
X02	10/03	34	change R3403 R3404 R3405 R3406 from ZZ.00PAD.M11 to 63.R0034.1DL	EMI request
X02	10/06	52	change EC5201 EC5202 from 78.6R864.1FL to 78.22034.1FL (22P)	EMI DMIC noise
X02	10/07	42	add EC4203 EC4204 (78.10422.5FL)	EMI DC_IN power noise
X02	10/07	63	del R6301 R6302 R6303 R6304; add TR6301 TR6302 ( 68.00201.201)	EMI USB2.0 noise
X02	10/08	86	add EC9725 EC9726 EC9727 EC9728 EC9729 (78.10422.5FL)	RF 25M noise
X02	10/08	86	add SPR4 (34.49026.001)	RF 25M noise
A00	10/28	24	change R2424 from 64.47025.6DL (47k) to 64.64925.6DL (64.9k)	PCB Version
A00	10/28	65	change DB1 from 20.D0075.110 to ZZ.00PAD.Y41	Dummy Pad with solder mask
A00	10/28	61	dummy PWRBT1	For X build
A00	10/30	18	dummy R1806 R1813 R1814 R1815	S3 leakage
A00	11/12	63	change CN6301 from 20.K0610.024 to 020.K0139.0024	FAE repair request
A00	11/13	24	change R2408 from ZZ.00PAD.M11 to 63.R0034.1DL & dummy	Synaptics Non PTP request
A00	11/13	62	dummy R6225	Synaptics Non PTP request
A00	11/17	11	add C1145 & dummy it	reserve for 1D05V power

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**Change History**

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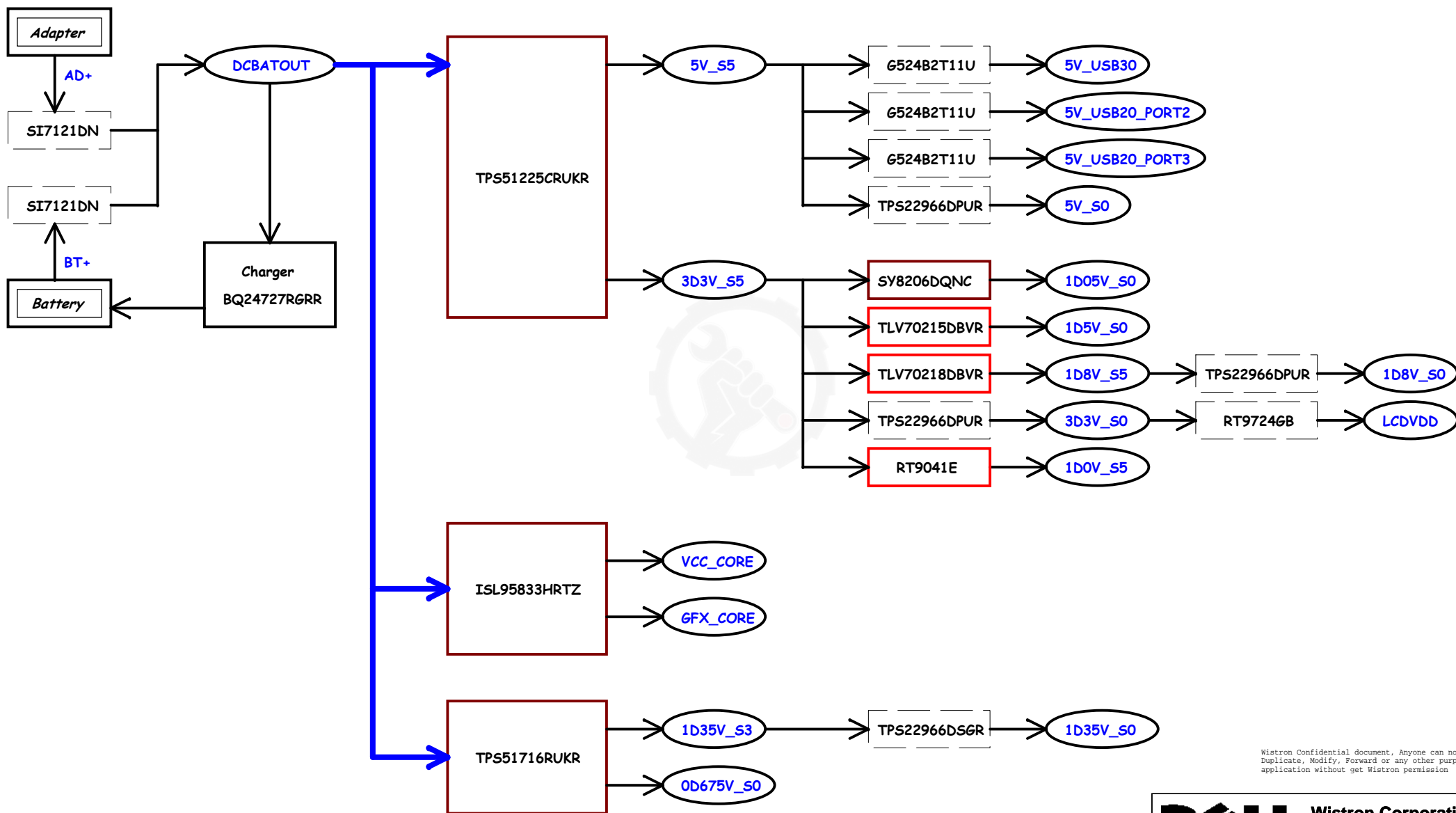
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# Power IC Type

Regulator

LDO

Load  
Switch



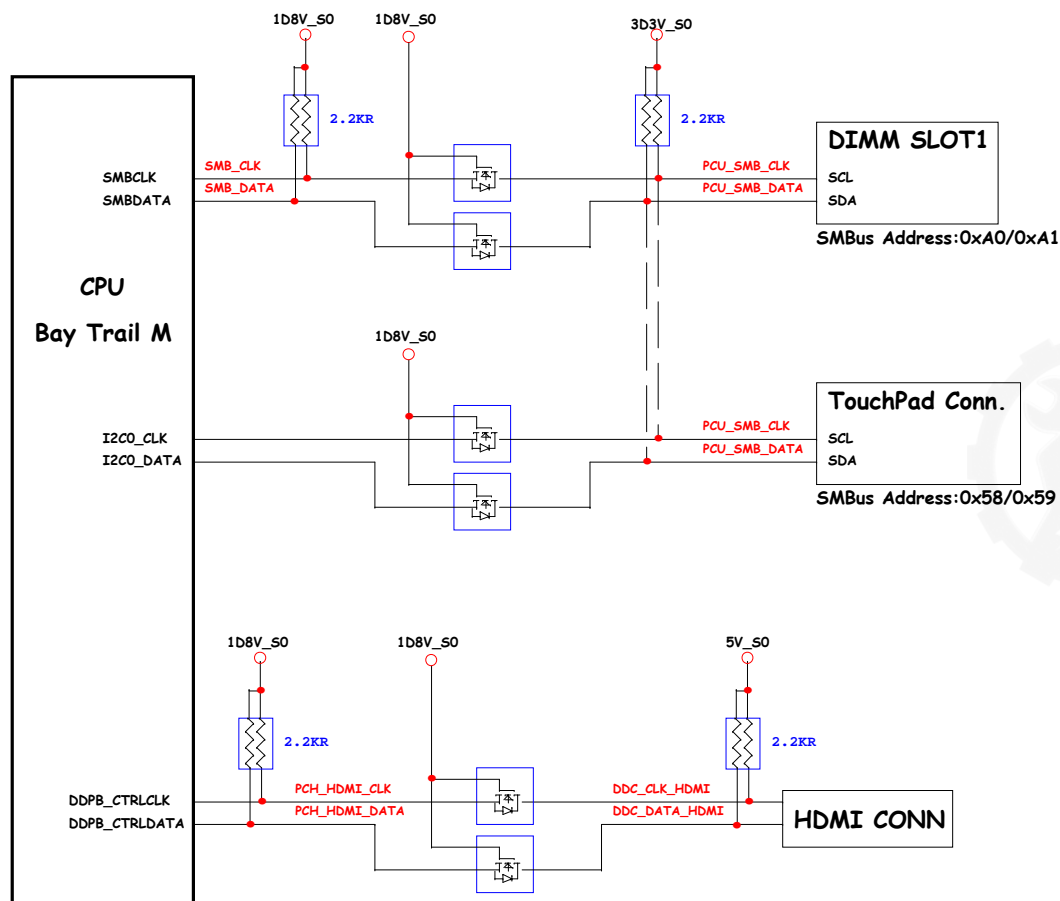
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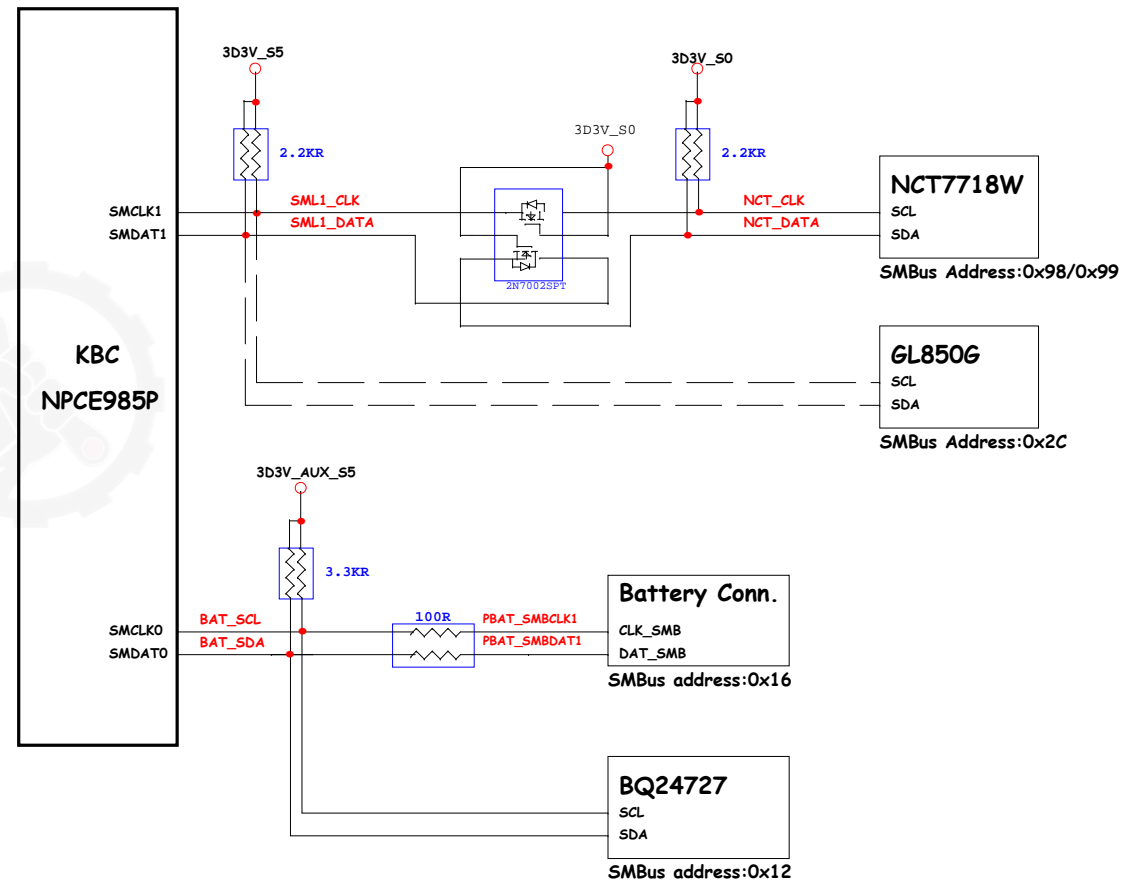
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Power Block Diagram		
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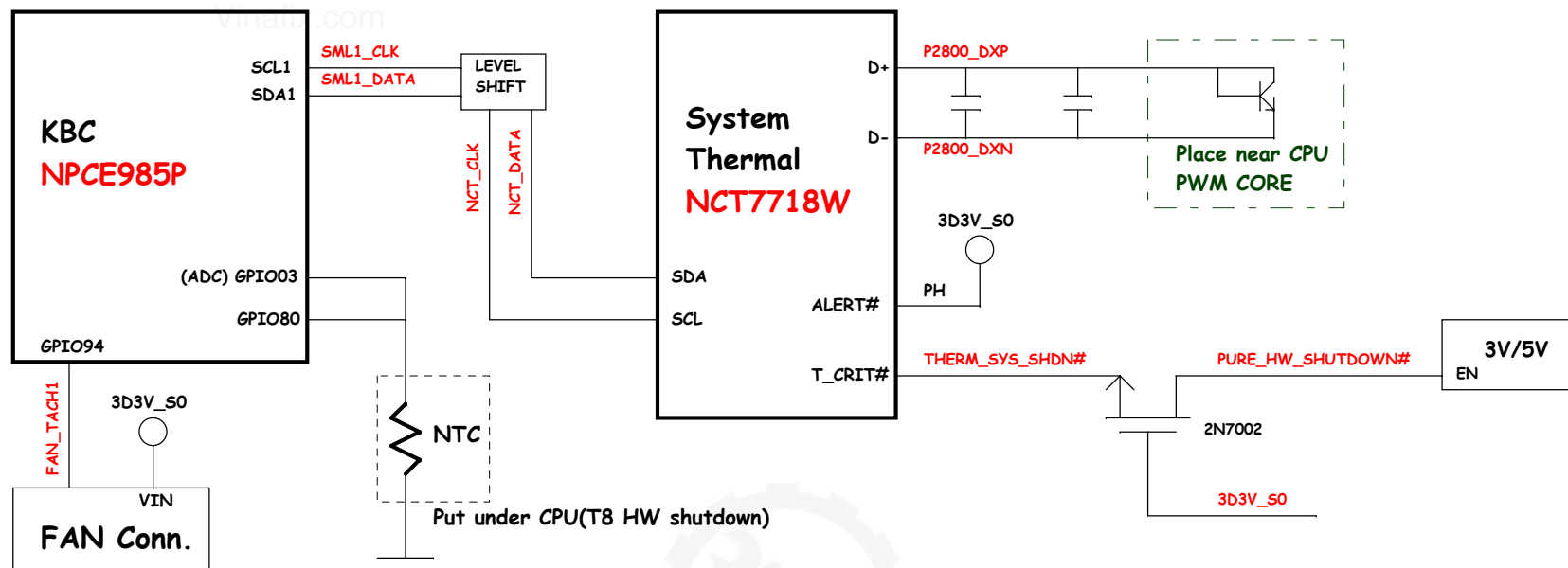
## CPU SMBus / I2C Block Diagram



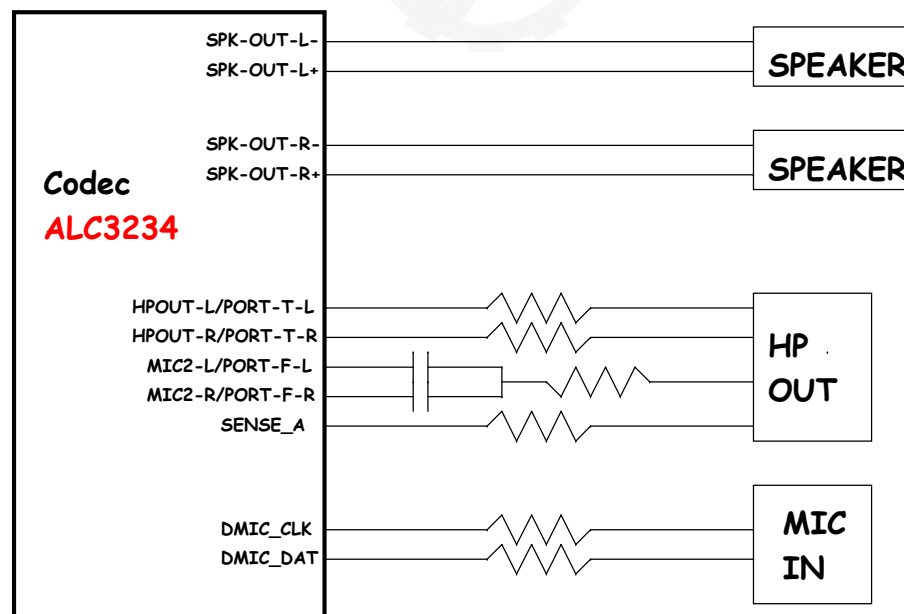
## KBC SMBus Block Diagram



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### Audio Block Diagram



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